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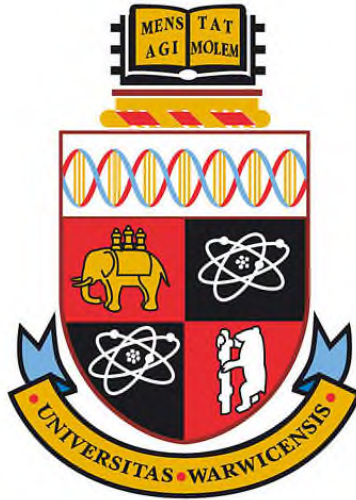
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Low Temperature Thermal Oxidation of Epitaxial 3C-SiC

By

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Thesis

Submitted to the University of Warwick

for the degree of Master of Science (MSc) by Research



Department of Physics

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I. Declaration

This thesis is submitted to the University of Warwick in support of the author's application for the degree of Master of Science by Research. Except where specifically stated, all experimental measurements were carried out by the author in collaboration with specialists.

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III. Abstract

Silicon Carbide (SiC) is a wide-bandgap semiconductor which has promising potential as a future material for power electronics devices such as metal-oxide-semiconductor field effect transistors (MOSFETs). The aim of this project was to take cubic SiC (3C-SiC) grown on silicon (Si) substrates by reduced-pressure chemical vapour deposition (RP-CVD) and investigate whether low-temperature ($< 1000\text{ }^{\circ}\text{C}$) dry oxidation is a suitable method for growing the dielectric oxide layers vital for device fabrication. To this end, heteroepitaxially grown 3C-SiC was oxidised at $985\text{ }^{\circ}\text{C}$ and a range of physical and electrical characterisation techniques were employed to assess the grown oxide.

X-ray reflectance (XRR) and cross-sectional transmission electron microscopy (X-TEM) analysis suggested a growth rate of around $4.08 \times 10^{-2}\text{ nm/min}$, comparable to that achieved on 4H-SiC. Qualitative analysis showed that this oxide closely followed the surface morphology of the 3C-SiC, and atomic force microscopy (AFM) proved that the oxide did not significantly alter the surface roughness of the as-grown 3C-SiC epilayers. X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) showed that the oxide had carbon (C) distributed inhomogeneously throughout the oxide, which may have served as charge traps at the oxide/3C-SiC interface and contributed to leakage through the oxide by trap-assisted tunnelling (TAT). The highest concentration of C was at the interface, totalling 25% of the material present.

Capacitance-voltage (CV), conductance-voltage (GV), and current-voltage (IV) analysis provided information about the electrical properties of the grown oxide. While a small inversion population was observed in the CV data, this quickly collapsed under negative bias. Relatively high leakage current through the oxide is the suspected cause of this. While leakage was high, the oxide/3C-SiC interface showed a relatively small interface state density (D_{it}) of $1 \times 10^{10}\text{ cm}^{-2}\text{eV}^{-1}$, which is comparable to that seen on similar material after post-oxidation annealing (POA), despite the fact that none was performed on this material. POA may further improve this D_{it} figure by up to an order of magnitude. In summary, this work provides some evidence that heteroepitaxially grown 3C-SiC is a viable material for power device applications, but optimisation of the oxidation method and post-oxidation treatment is required to make this material realise its full potential.

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VI. List of Abbreviations

AFM	Atomic force microscopy
BF	Bright-field
CCC	Closed-cycle cryostat
CVD	Chemical vapour deposition
CV	Capacitance-voltage
DF	Dark-field
D_{it}	Interface state density
DUT	Device under test
FCC	Face-centred cubic
FTIR	Fourier-transform infrared spectroscopy
GV	Conductance-voltage
IC	Integrated circuit
IGBT	Insulated-gate bipolar junction transistor
IPA	Isopropyl alcohol
IV	Current-voltage
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NIT	Near-interface trap
PAC	Photo-active compound
PE-CVD	Plasma-enhanced chemical vapour deposition
PMA	Post-metallisation annealing
POA	Post-oxidation annealing
RIE	Reactive-ion etching
RMS	Root mean square
RP-CVD	Reduced-pressure chemical vapour deposition
SIMS	Secondary ion mass spectroscopy
TAT	Trap-assisted tunnelling
TOA	Take-off angle
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectance
X-TEM	Cross-sectional transmission electron microscopy

1 Introduction & background

1.1 A brief history of semiconductor technology

The study of semiconductor technology can be traced back to the 19th century, long before the physical mechanisms that explain semiconductor behaviour were at all understood. Michael Faraday first reported a decrease in resistance of silver sulphide (Ag_2S) samples as they were heated, the opposite of the temperature dependence of the resistance of metallic samples¹. Others such as Becquerel, Smith, and Braun reported behaviour which we can now attribute to their samples being semiconductor materials, but as this research was prior to Thomson's discovery of the electron in 1897 the conduction mechanisms were not well understood². The early part of the 20th century showed huge development of solid-state theory, and by 1931 A. Wilson had developed the band theory of conduction, allowing for a much greater understanding of semiconductor behaviour³.

It can be argued that the true advent of the semiconductor era came with the invention of the point-contact transistor in 1947 by Bardeen, Brattain, and Shockley⁴. Their work earned them the Nobel Prize in 1956, but more importantly laid the foundation for an entirely new area of research into the applications of semiconductor technology. Bardeen, Brattain, and Shockley's transistor used germanium (Ge), as did most early transistors, however silicon (Si) soon overtook Ge as the dominant material for constructing semiconductor devices. It remains so to this day, although Ge is still used for certain applications where its properties are preferable⁵, as are several compound semiconductors such as silicon carbide (SiC), gallium arsenide (GaAs), gallium nitride (GaN) and silicon germanium (SiGe)⁶⁻⁸. This work focusses on SiC and its potential for high-power electronics.

Modern transistors are many orders of magnitude smaller than early attempts, and the development of semiconductor technology is often described in terms of either the size of transistors fabricated on integrated circuit (IC) chips, or how many transistors can be packed into a single chip. Famously, Gordon Moore, co-founder of Intel, postulated in 1965 that the number of components in a single IC would roughly double every year; he later revised this prediction to every two years which is the trend most commonly quoted^{9,10}. This prediction held until 2012, as increasingly small feature widths (the standard measure of device size, being the minimum length of the gate) require increasingly more

precise and complicated fabrication methods. Intel recognised 2012 and the 22 nm “node” as the point at which the trend of Moore’s law breaks down. As of 2018, the 7nm node has begun, with the widespread use of 7 nm technologies in processors such as the Apple A12, manufactured by the Taiwan Semiconductor Manufacturing Company (TSMC)¹¹. To date the smallest working transistor ever fabricated uses only a single atom, although it should be noted that the actual device that demonstrated this result was at the macro scale¹².

1.2 Semiconductors

A semiconductor can be defined simply as a material with a conductivity greater than that of an insulator, and less than that of a conductor. Their electrical resistance decreases with increasing temperature, rather than conductive materials (such as metals) in which increasing temperature will bring increasing electrical resistance. Semiconductor materials are usually crystalline, i.e. have a regular atomic structure that can be described in terms of a single repeated unit cell. In the case of 3C-SiC this unit cell takes the zinc-blende structure, which is shown in Figure 1.

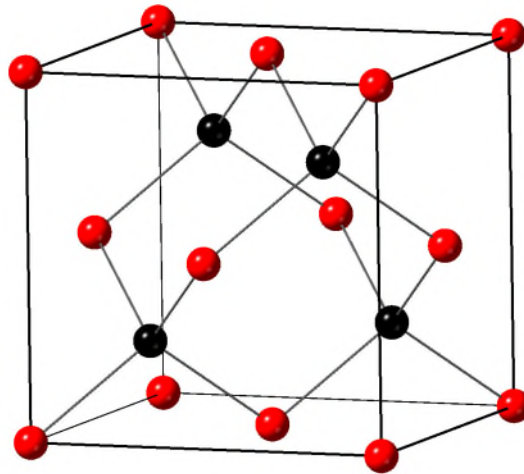


Figure 1: Unit cell of 3C-SiC. Si atoms are shown in red, C atoms are shown in black.

The zinc-blende structure has tetrahedral coordination: each Si or C atom’s four closest neighbours are of the other element, arranged in a tetrahedron. It can also be described as two interconnecting face-centred cubic (FCC) lattices (one Si, one C), where one lattice is offset by $\frac{1}{4}$ of the lattice constant along the (111) plane. Other polytypes of SiC have very different crystal structures, see section 1.4.

A semiconductor is often described in terms of its band gap; i.e. the energy required to raise an electron from the top of the highest energy band in which it is bound to its parent atom (*valence band*) to the bottom of the lowest energy band in which it can conduct freely within the crystal lattice of the bulk material (*conduction band*). In a semiconductor the Fermi level (the highest electron energy level when the material is at absolute zero) lies between the valence and conduction bands. For an intrinsic semiconductor, the Fermi level lies exactly halfway up the bandgap. This can be manipulated by doping the semiconductor.

Doping is the process by which impurities (dopants) are introduced into the crystal lattice to control the semiconductor's conductive properties. These are atoms which have either fewer valence electrons than the semiconductor material (known as an *acceptor* or p-type dopant) or more electrons than the semiconductor material (a *donor* or n-type dopant). As most semiconductors are Group IV elements, p-type and n-type dopants often come from Group III and Group V respectively. P-type dopants have fewer valence electrons in their outer shell than the semiconductor (3 in the case of Group III elements), meaning that they act as acceptor sites for electrons – the effect of this is that quasiparticles known as holes are created, which are free to travel about the crystal lattice in much the same way as electrons would (but of opposite charge, as a hole is by definition an absence of an electron so leaves whatever atom it is currently “bound” to with a net positive charge). The result of this is that the material has a net positive charge and is known as a p-type semiconductor. N-type dopants have more electrons in their outer shell than the semiconductor (5 for Group V) meaning that they provide a surplus of unbound electrons, giving the material a net negative charge; this is known as an n-type semiconductor. Doping with a p-type dopant will bring the Fermi level closer to the valence band edge, whereas doping with an n-type dopant will bring it closer to the conduction band edge.

We can further classify semiconductors as having either a direct or an indirect bandgap. In order to understand this we can describe the semiconductor in terms of its Brillouin zones. The Brillouin zones are the reciprocal of the Bravais lattice we use to describe the crystal structure of a material in real space; in other words, it is a representation of the lattice in momentum space (often called *k-space*). Direct bandgap semiconductors are those in which there is no difference in the k-vector between the extrema of the valence and conduction bands (see Figure 2); i.e. the highest energy point of the valence band and the lowest energy point of the conduction band have the same k-vector. In order for an

electron to transition from the valence to the conduction band in such materials all that is required is that the energy imparted to the electron exceeds the band gap of the material. In practical terms this means that direct bandgap semiconductors such as GaAs are often very good materials to use in solar cells or light-emitting diodes (LEDs) as photon emission can be stimulated with a relatively low current. The bandgap of GaAs (1.42 eV) means that it is often used to make infrared LEDs¹³.

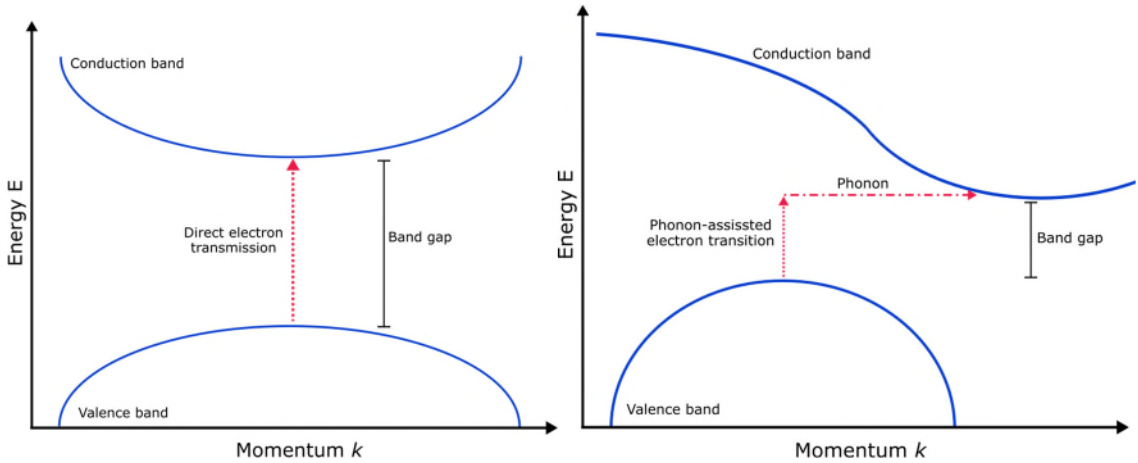


Figure 2: Direct bandgap (L) and indirect bandgap (R) represented in momentum space k . For an electron transfer to occur in an indirect bandgap semiconductor a phonon must also occur and cause a change in momentum.

By contrast indirect bandgap semiconductors are ones in which there is a difference in k -vector between the valence and conduction bands. It is therefore necessary for a phonon to provide momentum to the electron which coincides with an excitation in order for the electron to transition between bands. Indirect transition is consequently far less likely to occur than direct transition.

1.3 Power devices & their applications

Novel materials for power devices are a burgeoning area of research as the physical limits of what is possible with traditional Si devices are reached. Power devices are used in a very broad range of applications including consumer electronics, automotive electrical systems, telecommunications, and high-voltage power transmission. Current and voltage ratings for these products can vary from tens of volts or several amps all the way to tens of kV and kA¹⁴. Applications such as high-voltage transformers can require blocking voltages of hundreds of kV, which are currently achieved by using several Si devices connected in series; clearly there is opportunity for a single device to replace these arrays. There are promising indications that wide-bandgap semiconductors such as SiC may be

a more efficient solution. The maturity of Si technology is also somewhat of a barrier to revolutionary breakthroughs, so exploring novel or more niche materials such as wide-bandgap semiconductors may yield more unexpected solutions.

Chief among all power electronics devices are the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and the insulated gate bipolar transistor (IGBT). Both of these devices require a dielectric layer, which for Si is usually SiO₂. SiC a promising alternative in part because similar techniques for oxidation can be applied to SiC as are used for Si, and SiO₂ can be grown natively on SiC. There are a number of challenges to overcome however before SiC can become a widely adopted alternative to SiC, as often the oxides grown on SiC have a higher interface state density (D_{it}) which can greatly affect device performance. These devices also require a low on-resistance, low leakage current, and fast switching speed in order to function effectively in a power electronics application.

At their most basic, transistors are semiconductor devices which allow an electrical signal to be switched or amplified. MOSFETs are transistors which exploit the charge accumulation properties of a MOS-stack (as described in section 2.2) in order to perform this switching. Typically this consists of a body (sometimes known as a substrate but referred to as body here to differentiate from epitaxial substrate) of either p- or n-type semiconductor with two regions composed of semiconductor with the opposite charge (e.g. two n-type regions embedded in a p-type body) ¹⁵. The two embedded regions are known as the source and the drain and are capped with metal contacts. In between these contacts, and on top of the body material, a layer of oxide is grown which electrically insulates the source and the drain from one another. Crucially the oxide is a dielectric medium, meaning that it is electrically insulating but in the presence of an electric field will become polarised. This oxide layer is also capped with a metal contact, known as the gate. Figure 3 shows a diagram of a conventional MOSFET. Many other designs exist for specific applications, but all operate using similar principles ¹⁴.

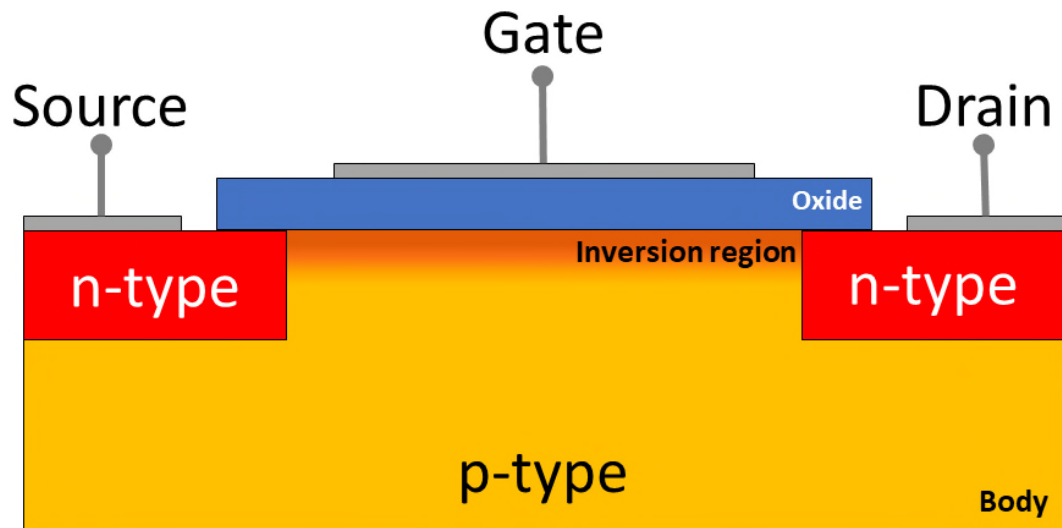


Figure 3: Cross-sectional diagram of a conventional MOSFET device.

As a voltage is applied to the gate (the gate voltage, V_G), the MOS stack formed by the gate, the oxide, and the body undergo the accumulation, inversion, and depletion behaviours described in section 2.3. When an inversion region is formed, this allows current to flow between the source and the drain as this inversion region now has the same charge type as the source and drain regions. Therefore, by varying the gate voltage the flow of current can be directly controlled.

The suitability of a MOSFET for a specific application is dependent on a number of performance factors. Blocking voltage, the maximum voltage that can be applied before the device fails (i.e. the oxide layer becomes electrically conductive), is one such factor and particularly for power electronics MOSFETs are often rated by their blocking voltage. Closely linked to this is the critical breakdown electric field strength, which is the strength of electric field which a given MOSFET can withstand before it fails – this will vary depending on the doping level of the semiconductors. On-resistance – the resistance of the device when the inversion region is formed and the source and drain are connected – is also of great importance and for most purposes the ideal on-resistance is zero. This is of course impossible to achieve but MOSFET device manufacturers try to minimise on-resistance as much as possible. The quality of the oxide layer is of paramount importance for most of these factors. Poor quality oxide can have a high leakage current, which is the current that is able to pass through the oxide. As with on-resistance the leakage current is minimised as much as possible as leaky oxides will result in devices which are inefficient and causes issues with correctly forming and maintaining the inversion state ^{16,17}.

MOSFETs tend to have a much greater switching speed than IGBTs and a lower on-resistance, and so have been the focus of a lot of attention in recent years ^{18,19}. SiC is in theory an ideal material for high-power MOSFET as it has a relatively low on-resistance, a high critical breakdown electric field strength, and has a voltage blocking region ten times smaller than that of Si for the same blocking voltage, meaning that a fast switching speed is usually fairly easy to achieve ^{20,21}.

1.4 Silicon carbide

SiC is a wide-bandgap semiconductor with promising potential as a replacement for Si in high-temperature, high-power and high-frequency devices. It also has an indirect bandgap. Recent work ²² has shown increased interest in the use of SiC in power electronics devices, particularly using the sole cubic polytype 3C-SiC and hexagonal polytypes 4H-SiC and 6H-SiC. 3C-, 4H-, and 6H- are the most commonly used polytypes of SiC and their different crystal structures cause significant differences in their physical parameters, most pertinently their bandgaps. 3C-SiC is the sole cubic polytype of SiC, while 4H- and 6H-SiC are both examples of hexagonal polytypes. In total over 200 polytypes of SiC are known to exist, although not all are well understood ²³. All polytypes of SiC are stacked in hexagonal frames of bilayers. The numerical designation of each polytype corresponds to the length of the stacking sequence of these bilayers; (ABCABC...) for 3C-SiC, (ABCBABCB...) for 4H-SiC, etc ²⁴. Figure 4 shows the stacking sequence for 3C-SiC, 4H-SiC, and 6H-SiC, on the (001) and (11 $\bar{2}$ 0) planes respectively.

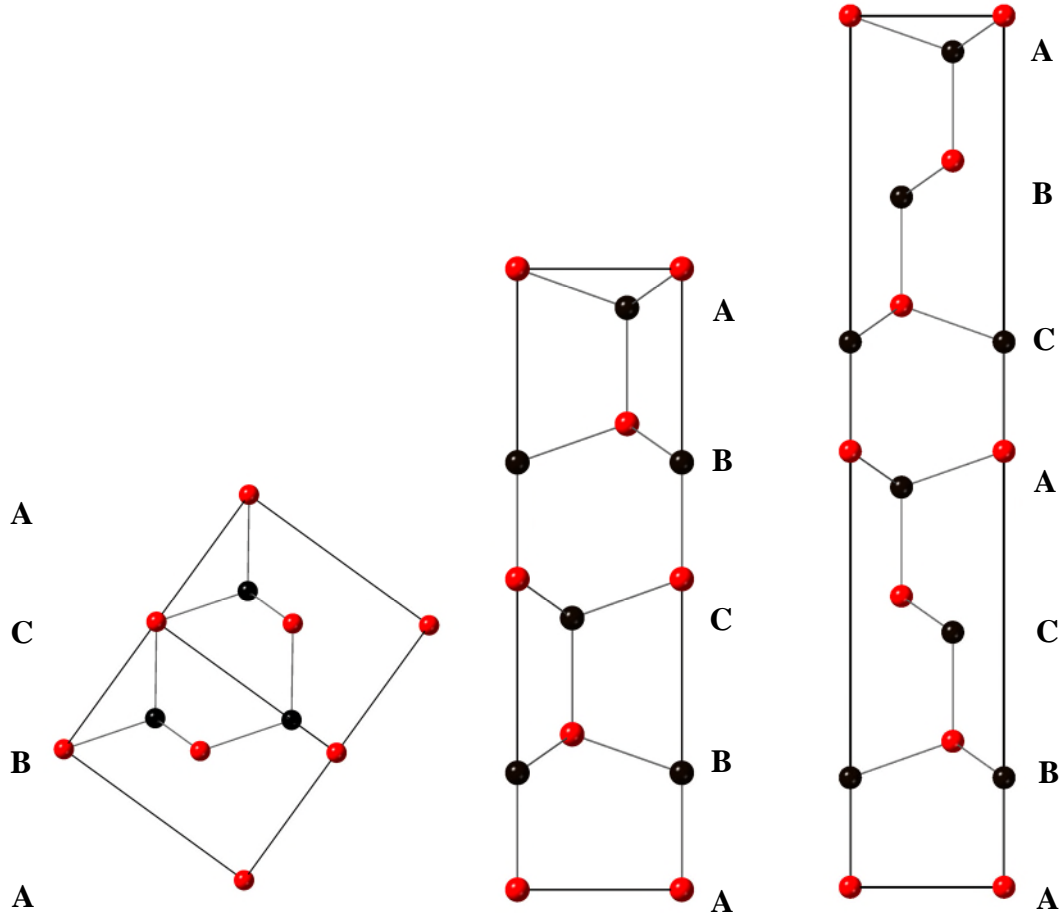


Figure 4: Stacking sequence of 3C-SiC (L), 4H-SiC (C) and 6H-SiC (R).

3C-SiC has a number of advantages over both Si and 4H-SiC which make it an exciting prospect for future devices. The principal advantage over 4H-SiC is cost: 3C-SiC can be grown by heteroepitaxy on Si substrates, which are significantly cheaper than the 4H-SiC substrates required for homoepitaxial growth²⁵. 3C-SiC also has a slightly smaller bandgap than 4H-SiC (2.36 eV compared to 3.23 eV²⁶) meaning that 3C-SiC Metal-Oxide-Semiconductor (MOS) devices should theoretically be preferable as there would be fewer available interface states in the bandgap, leading to a greater field-effect mobility of electrons or holes in the inversion channel²⁷.

Many polytypes of SiC are preferable to Si for specific applications as they can withstand significantly higher temperatures; Si melts at 1414 °C²⁸, whereas 3C-, 4H-, and 6H-SiC melt at around 2830 °C²⁹. As such SiC-based devices could be used in places where Si components could not function, for example as gas or temperature monitoring sensors in the high-temperature exhausts of power plants. SiC's higher critical breakdown strength is also very advantageous as this suggests that SiC devices could withstand much higher voltages than Si; meaning that they are ideal for power electronics applications.

Recent work has shown that SiC MOSFETs can withstand a blocking voltage approximately one order of magnitude higher than Si³⁰; in time novel device structures may be developed that pushes this even higher. In the case of 4H- and 6H-SiC, these polytypes are often grown by homoepitaxy, but (as in this work) 3C-SiC is often grown by heteroepitaxy on Si substrates. It would therefore be necessary to remove the Si substrate while retaining the 3C-SiC epilayer to take advantage of the high-temperature and high-power benefits.

There are however several challenges to overcome before SiC can overtake Si as the “go-to” material for power electronics applications. Firstly, it must be demonstrated that high-quality oxides can be grown on SiC. MOS technology is essential in all aspects of modern electronics, and SiO₂ on Si growth is very well understood. While recent work has shown interest in 4H- and 3C-SiC oxidation, grown oxides are generally of poorer quality than that which is possible on Si, with interface state densities several orders of magnitude larger^{27,31,32}. This contributes to leakage across the oxide and would impact device performance. This project attempts to demonstrate that high-quality oxides can be grown on 3C-SiC at temperatures below 1000 °C. If this is possible, it would potentially reduce the cost of manufacturing MOS-based 3C-SiC devices as oxide growth is a time consuming and expensive process. Any reduction in the oxidation temperature will result in a cheaper fabrication process, simply because the energy demands of the oxidation furnaces will be lower. Oxidation rate is highly dependent on temperature³³, so there is a balance to be struck between a lower-temperature oxidation which requires more time, and higher-temperature oxidation that is quicker but requires hotter furnaces.

The main alternative to SiC as a power electronics material is GaN. SiC and GaN are both wide-bandgap materials, making them suitable for applications where devices are required to operate at high temperatures or in applications requiring high electric breakdown fields. Both materials have similar electric breakdown properties, having blocking voltages of between 46-56 and 34 times that of Si respectively³⁴, which makes them both attractive alternatives to Si in devices such as HVDC transformers. GaN also has a similar bandgap to 4H- and 3C-SiC at 3.45 eV³⁵; however crucially GaN has a direct bandgap which makes it more suited to optical devices such as ultraviolet LEDs³⁶. The great advantage that SiC has over GaN is that it has a much greater thermal conductivity, meaning that loss of device performance with increasing temperature is much less of a concern. Again this would require either using homoepitaxial SiC or the

removal of any substrate (such as Si). Commercially available GaN devices typically require a heat sink to dissipate excess heat and have been shown to have a much greater on-resistance with elevated temperature³⁷. In general SiC is also easier to dope than GaN, with a higher controllability of dopant concentration. It is also worth noting that SiC has been explored as a virtual substrate material for GaN³⁸ and so for certain applications these materials together may be the optimal solution. A virtual substrate is an epilayer grown on a substrate to act as a substrate for a second epilayer.

For this work the most pertinent advantage of SiC over GaN is that it can form a native oxide (SiO₂), as discussed in section 1.3. Being able to grow oxide directly on the as-grown SiC allows MOS-based devices (most often MOSFETs) to be fabricated with relative ease and through use of simple methods such as the dry thermal oxidation used in this work. To date the majority of SiC power devices have used 4H-SiC due to its wide availability and relatively low cost²⁰. There is however space for a lower-cost, easy to grow alternative in the heteroepitaxial 3C-SiC discussed herein.

1.5 Low-temperature 3C-SiC epitaxy

This project builds on the work by Gerard Colston over the course of his PhD, which demonstrated that 3C-SiC could be grown heteroepitaxially atop Si substrates, at low temperatures in a conventional Chemical Vapour Deposition (CVD) reactor²⁵. All of the material used in this research has been grown by reduced-pressure chemical vapour deposition (RP-CVD) in the ASM Epsilon 2000 RP-CVD reactor located at the University of Warwick^{39,40}. This reactor is the first industrial-level reactor installed in a UK university. RP-CVD is one of several forms of epitaxy, a process by which crystalline layers are deposited one by one atop another crystalline material. Where this material exists purely for the deposition of layers on top of it, it is known as a substrate. The deposited material is known as an epilayer. Epilayers can range from a single atomic layer (often known as monolayers) up to hundreds of microns in thickness. Other epitaxial methods include molecular-beam epitaxy (MBE) and variants of CVD such as plasma-enhanced chemical vapour deposition (PE-CVD) and thermal CVD⁴¹⁻⁴³.

MBE can be advantageous for growing monolayers as it has very high controllability; the downside to this is speed. MBE is a very time intensive process which requires a very high vacuum in order to operate effectively⁴⁴. The reproducibility of wafers is also often

quite poor (despite the high controllability). The epilayers grown for this project were on the order of hundreds of nanometers in thickness, so although only a relatively small amount of material was required, MBE was not the most suitable method. RP-CVD offers the required deposition control at a greatly enhanced speed and reduced cost. The downside to CVD growth is that it often requires growing many wafers in order to calibrate the equipment; once this is done reproducibility is typically very good, but the calibration wafers are of little to no use.

Chief among all commercial epitaxy is Si, which is the most common substrate material and is by far the cheapest to produce. Si wafers can also be grown at much larger sizes (approximately 450 mm diameter) than other substrate materials. All the 3C-SiC used in this work has been grown by heteroepitaxy on 100 mm diameter Si substrates because of Si's market dominance; if high-quality 3C-SiC can be grown on Si and devices fabricated from it, the relative cost of 3C-SiC technologies will be significantly reduced. This will make 3C-SiC a much more attractive product for power electronics devices. Grown on Si substrates also usually means that pre-existing technologies and techniques currently used for Si – such as RP-CVD, B and P as dopants, etc. – can be used with 3C-SiC, further increasing its attraction as a commercial product.

The work of Colston et al. has shown that high-quality, fully relaxed 3C-SiC can be grown by RP-CVD on Si substrates up to 100 mm in diameter³⁹. Crucially for device fabrication this material can be grown hundreds of nanometres thick with very little wafer bow. This means that it is possible to use almost the entire wafer to make devices, bringing the overall cost per device down significantly. Wafer bow is the amount to which a grown epilayer causes the substrate wafer to bend and is measured as a deviation from the “ideal” flat wafer⁴⁵. The causes of wafer bow are typically lattice mismatch – the percentage difference between the lattice constant of the epilayer material and the substrate material – and differences in thermal expansion coefficients of the epilayer and substrate. Both of these factors will cause strain in the material, causing it to bend.

Due to the relatively large lattice mismatch (19.7% at room temperature) and difference in thermal expansion coefficient (~8% at room temperature)⁴⁶, issues such as wafer bow can cause difficulties in the heteroepitaxy of 3C-SiC on Si. Recent work has shown significant improvement in this area as material grown at lower temperatures by industry standard RP-CVD can significantly reduce wafer bow while maintaining high crystal

quality and very low surface roughness (<2 nm) ^{39,40}. Surface roughness and its quantification are discussed in section 4.1.3.

2 Theory and methodology

2.1 Oxidation chemistry

Much has been written on the oxidation of Si, but perhaps the definitive reference text is *General Relationship for the Thermal Oxidation of Silicon* by B. E. Deal and A. S. Grove ³³. In this paper Deal and Grove outline their Deal-Grove model, which at the time was the most complete picture of how Si oxidises and laid the foundation for several different corrective models. While this thesis will not repeat the full details of the paper, it is important to consider the basic premises set out therein. The oxidation of SiC has been shown to be qualitatively similar to that of Si, so understanding the basics of Si oxidation is valuable in interpreting the data presented in this work.

The Deal-Grove model states that the oxidation of Si is essentially steady-state, and controlled by three flux values F_1 , F_2 , and F_3 . Respectively they are:

1. F_1 , the flux of the oxidant from the gas to the outer surface of the oxide, being;

$$F_1 = h(C^* - C_O) \quad (1)$$

where h is the gas-phase transport coefficient, C^* is the equilibrium concentration of ambient oxidants, and C_O is the concentration of oxidants at the oxide surface.

2. F_2 , the flux of the oxidant across the oxide layer, being:

$$F_2 = D_{eff} \left(\frac{C_O - C_i}{x_0} \right) \quad (2)$$

where D_{eff} is the effective diffusion coefficient, C_i is the concentration of oxidant at the oxide/silicon interface, and x_0 is the thickness of the oxide. This equation is obtained by assuming a steady state condition of Fick's law:

$$F = -D_{eff} \left(\frac{dC}{dx} \right) \quad (3)$$

3. F_3 , the flux corresponding to the oxidation reaction:

$$F_3 = kC_i \quad (4)$$

where k is the rate constant associated with the consumption of oxidants in the reaction at the oxide/silicon interface.

In the steady-state condition these three flux values are assumed to be equal, hence the flux can be expressed by a single value F , given by

$$F = F_1 = F_2 = F_3 = \frac{kC^*}{1 + \frac{k}{h} + \frac{kx_0}{D_{eff}}} \quad (5)$$

Note than for this to be valid we assume that the diffusivity is very small relative to k and h , which brings C_i approaching 0 and C_o approaching C^* . If we then introduce N_1 , the number of oxidant molecules per unit volume of the oxide layer, we can obtain the following expression for the growth rate from equation (5):

$$\frac{dx_0}{dt} = \frac{F}{N_1} = \frac{\frac{kC^*}{N_1}}{1 + \frac{k}{h} + \frac{kx_0}{D_{eff}}} \quad (6)$$

Where t is equal to time and all others are as above. Any Si surface in atmosphere will have a native surface oxide of thickness x_i , so if we introduce the condition $x_0 = x_i$ at $t = 0$, and solve equation (6) by integration we get

$$x_0^2 + Ax_0 = Bt + x_i^2 + Ax_i \quad (7)$$

commonly rewritten as

$$x_0^2 + Ax_0 = B(t + \tau) \quad (8)$$

here $\tau \equiv \frac{x_i^2 + Ax_i}{B}$, which is a compensation for the initial oxide thickness x_i . We can then solve the quadratic equation (7) for x_0 , which yields perhaps the most useful expression for oxide thickness:

$$\frac{x_0}{A/2} \cong \left(\frac{t}{A^2/4B} \right)^{\frac{1}{2}} \quad (9)$$

As the Deal-Grove model is so widely accepted many papers consider only the so-called linear and parabolic rate constants when describing various oxidation methodologies.

These coefficients are usually derived from equation (9) and are individually valid for different regimes. For the initial oxidation, i.e. when $t \ll \frac{A^2}{4B}$, we consider the linear rate constant

$$\frac{B}{A} = \frac{kh}{k+h} \left(\frac{C^*}{N_1} \right) \quad (10)$$

i.e. for the initial oxide growth, the growth rate is linear. We can define the oxide thickness as

$$x_0 \cong \frac{B}{A} (t + \tau) \quad (11)$$

for the linear regime. For longer oxidation times when $t \gg \frac{A^2}{4B}$, we consider B alone, where

$$B = \frac{2D_{eff}C^*}{N_1} \quad (12)$$

and hence the oxide thickness is given by

$$x_0 \cong \sqrt{Bt} \quad (13)$$

Put simply, the oxidation is linear for thin oxides and after a critical point becomes parabolic in nature; thus the Deal-Grove model is often referred to as the linear-parabolic growth model. While this model was extremely useful for the early days of semiconductor engineering when oxides in excess of 30 nm were commonplace in semiconductor devices, as time went by devices became increasingly small and hence oxides became thinner, the shortcomings of the model became apparent. The model closely matches experimental data for thicker oxides, but anything less than around 30 nm diverged from the expected behavior. Deal and Grove also note within their work that the parabolic regime is difficult to model and doesn't always provide an accurate approximation.

In 1985 Massoud et al. proposed a correction to the Deal-Grove model, introducing exponential terms that describe the growth of thin films (<30 nm)⁴⁷. This study involved the dry oxidation of Si at temperatures between 800 and 1000 °C. Oxidation rate by the Massoud correction is given by the equation

$$\frac{dx_0}{dt} = \frac{B}{2x_0 + A} + C_1 e^{-\frac{x_0}{L_1}} + C_2 e^{-\frac{x_0}{L_2}} \quad (14)$$

where the B and A are as described by the Deal-Grove model and the constants C_1 and C_2 together with their respective characteristic lengths L_1 and L_2 (being thicknesses of grown oxide) define the correction for the thin film regime⁴⁸. Each exponential term decays with increasing oxide thickness. For sufficiently thick oxides (approximately 25 – 30 nm) the growth is entirely linear-parabolic as described by the Deal-Grove model⁴⁹.

The oxidation rate can also be expressed such that the exponential terms decay with time rather than with oxide thickness;

$$\frac{dx_0}{dt} = \frac{B + K_1 e^{\left(\frac{-t}{\tau_1}\right)} + K_2 e^{\left(\frac{-t}{\tau_2}\right)}}{2x_0 + A} \quad (15)$$

where the K -and τ -parameters can be expressed as Arrhenius expressions (i.e. can be plotted on a log scale as straight lines):

$$K_x = K_x^0 e^{-\left(\frac{E_{Kx}}{kT}\right)} \quad (16)$$

$$\tau_x = \tau_x^0 e^{-\left(\frac{E_{\tau x}}{kT}\right)} \quad (17)$$

where E_{tx} are the activation energies of the two exponential components. Massoud et al. discuss how both the activation energies and the various exponential coefficients (K_x , τ_x , C_x) differ with both temperature and crystal orientation. In this work a single oxidation temperature (985 °C) and crystal orientation (100) were used. Equivalent parameters were not calculated, as the oxidation of Si and SiC is not identical, however it is useful to consider the effect of orientation and temperature on the oxidation rate in a qualitative sense.

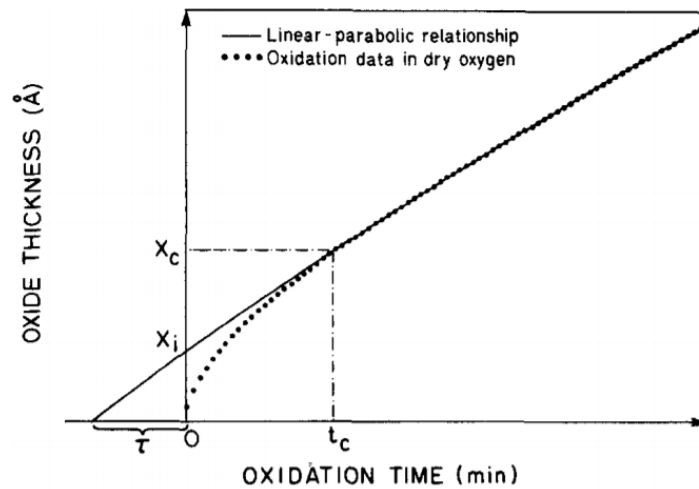


Figure 5: Massoud correction to the Deal-Grove model, fit showing the linear-parabolic relationship between oxide thickness and oxidation time. Reproduced from⁵⁰.

The equivalent mechanism for SiC oxidation was described by Song et al.⁵¹. This is a correction to the Deal-Grove model, adding in additional terms to describe the transport of product gases (namely CO) through the oxide film and their removal from the oxide surface. The theoretical model is non-specific as to the SiC polytype, but Song et al. apply it experimentally to 4H-SiC on the (0001) Si, (0001) C, and (1120) *a* faces. They show that the oxidation of 4H-the difference in oxidation rates on different crystal faces is an order of magnitude larger than for Si. Oxidation by Song et al. was performed using ambient dry oxygen at temperatures between 950-1150 °C, which helped to inform the decision to investigate similar temperatures in this work.

The additional terms which the Song model adds relate to the transport of CO through the oxide layer, and to the forward and reverse reactions at the SiO₂/SiC interface. The flux F at this interface can be described by

$$F = K_f C_{O_2} - K_r C_{CO} \quad (18)$$

where K_f and K_r are the forward and reverse rate constants, and C_{O_2} and C_{CO} are the concentrations of O₂ and CO at the interface. Experimentally it was shown that K_f is related to the local concentration of C in 4H-SiC. As all of the material used in this research was (001)-oriented 3C-SiC, all surfaces were Si-terminated. A steady-state condition is assumed for the oxidation, as with the Deal-Grove model, where $F:F_{O_2}:F_{CO} = 1:1.5:1$. The authors propose that the growth rate of the oxide layer is described by

$$\frac{dx_0}{dt} = \frac{F}{N_0}, \quad (19)$$

(where N_0 is the number of oxidant molecules incorporated into a unit volume of the oxide layer⁵¹) and hence from equation (19) this growth must be dependent on the diffusion rates of both the oxygen transport into, and CO transport out of, the oxide layer. As CO is a particularly stable molecule, it is necessary for it to transport out of the oxide rather than being broken down and the oxygen reincorporated into the oxide layer. This is outlined by equation (18) where F is dependent on C_{CO} . Figure 6, reproduced from⁵¹, shows diagrammatically the stages of O₂ and CO transport considered.

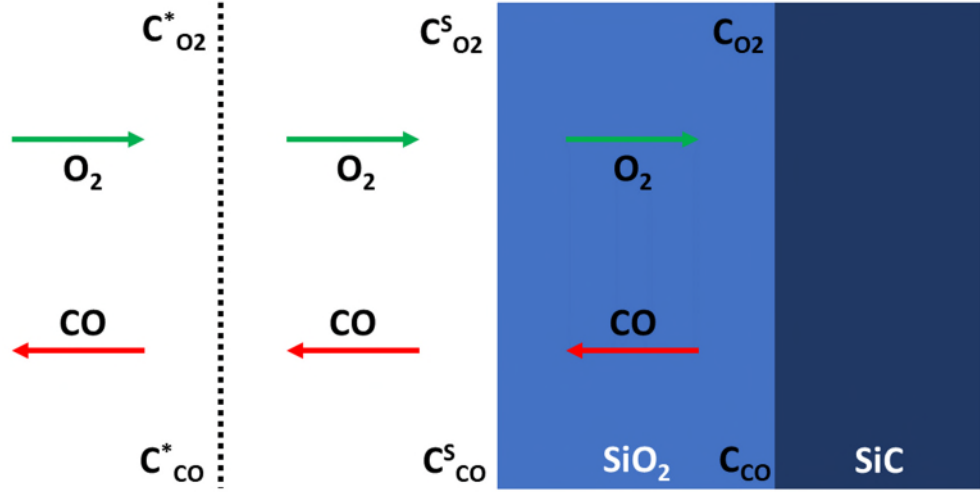


Figure 6: Representation of oxide transport across sample interfaces. Symbols retain their meanings as described in equations 17-20. Reproduced from ⁵¹

The rate constants A and B from Deal-Grove can be redefined in relation to these additional constants. As previously the rate-controlling step is dependent on whether the growth regime in question is linear or parabolic. In the linear regime the growth rate is controlled by the interface reaction and hence we consider B/A :

$$\frac{B}{A} \approx \frac{C_{O_2}^*}{N_0} K_f \quad (20)$$

In the parabolic regime the growth rate can be controlled either by O_2 diffusion into the oxide layer or CO diffusion out from it; respectively this gives us the rate constant B as:

$$B \approx \frac{C_{O_2}^*}{1.5N_0} D_{O_2} \quad (21)$$

$$B \approx \frac{C_{O_2}^* K_f}{N_0 K_r} D_{CO} \quad (22)$$

where $C_{O_2}^*$ is the equilibrium concentration of O_2 , N_0 is the number of oxidant molecules per unit volume of the oxide, D is the gas diffusion coefficient (distinguished by subscripts) and all other symbols retain their meanings. Whether O_2 or CO diffusion is the majority contributor to the growth rate is determined by the ratio of the forward and reverse rate constants. If $K_f/D_{O_2} \gg K_r/D_{CO}$, O_2 diffusion will dominate, if the reverse, CO diffusion will dominate.

2.2 MOS device structure & capacitance

Metal-Oxide-Semiconductor (MOS)-based devices are widely used for a wide variety of applications, many involving significantly more complicated structures than those detailed herein. For the purposes of initial characterisation however a simple MOS-stack as shown in Figure 17 is often used to assess the quality of a dielectric layer. For this research, MOS-stacks of the same approximate dimensions were fabricated on oxides of various thickness such that the capacitance and other parameters of the grown oxide layers could be assessed (see section 2.3). Principal among these techniques were CV and GV sweeps.

In order to analyse gathered data and assess the desired characteristics of the dielectric layer, it is important to understand the physical mechanisms happening inside the MOS layers as carriers are moved by an applied external electric field (i.e. a gate voltage). Three main regimes are seen in any C-V sweep: *accumulation*, *depletion*, and *inversion*. Accumulation occurs when the applied gate voltage causes majority carriers to build up at the interface between the semiconductor and the dielectric; in this case the 3C-SiC and the grown oxide. The 3C-SiC was not intentionally doped, but C-V data suggested that it was lightly n-doped with N. Therefore we will consider an n-type semiconductor for the purpose of this example. P-type MOS stacks will behave in a similar way but of course the majority and minority carriers will be the opposite and hence the C-V sweep appears reflected vertically as shown in Figure 7.

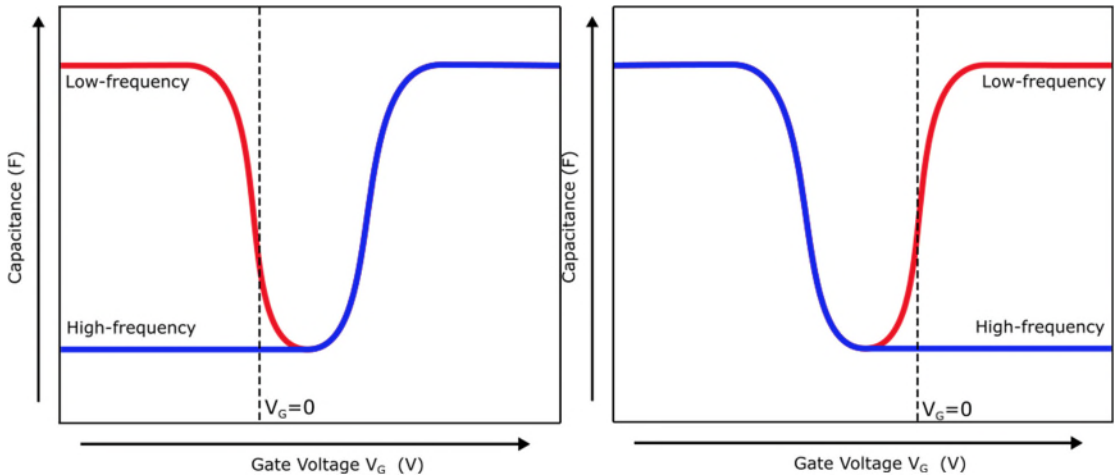


Figure 7: Ideal CV profiles for p-type semiconductor (L) and n-type semiconductor (R). Frequency dispersion is only seen in the inversion region.

In the n-type semiconductor, electrons accumulate at the semiconductor/oxide interface (in the semiconductor's valence band) when a positive gate voltage is applied. This is

caused by a deficit in electrons (therefore a net positive charge) at the metal/oxide interface from the applied voltage as in any standard capacitor. In terms of the C-V response, during accumulation we see the maximum possible capacitance of the device under test (DUT), which will appear essentially flat. It is from this region that we extract the oxide thickness value. The accumulation of charge causes what is known as band bending, as in seen in Figure 8. This is the change of the effective valence and conduction band energies of the semiconductor close to the oxide surface. In this instance we also see lowering of the valence and conduction band edges of the oxide.

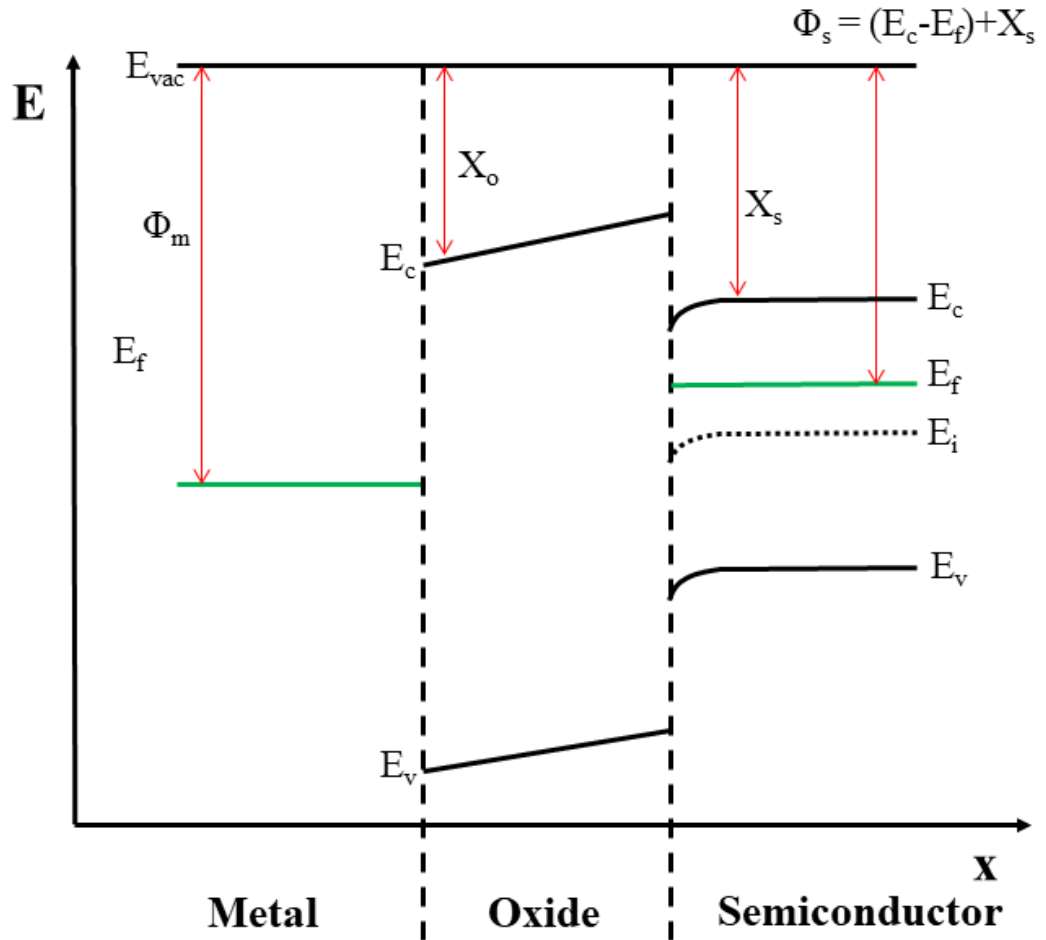


Figure 8: Accumulation condition for a metal (M) oxide (O) semiconductor (S) stack. Valence, intrinsic, and conduction band edges are shown (E_v , E_i , E_c) along with the Fermi level (E_f) and vacuum energy (E_{vac}). X_o and X_s are the electron affinities for the oxide and semiconductor respectively. Φ_s is the work function of the metal.

As the C-V sweep continues into a small negative applied bias, the MOS-stack will enter the depletion regime (Figure 9). Here, the net negative charge at the metal contact causes the region which was previously accumulating electrons to begin to expel electrons down into the semiconductor, leaving positively charged ions at the semiconductor/oxide

interface. The depletion region is so named as it has been depleted of majority carriers (i.e. electrons). The ions are immobile charges, and as the majority carriers have been depleted the region cannot conduct charge, effectively becoming a dielectric like the oxide. We also observe band bending in the opposite direction to accumulation, with the valance and conduction bands of the semiconductor now bending upwards (i.e. higher energy). The depletion region will increase in thickness with an increasingly large negative gate voltage.

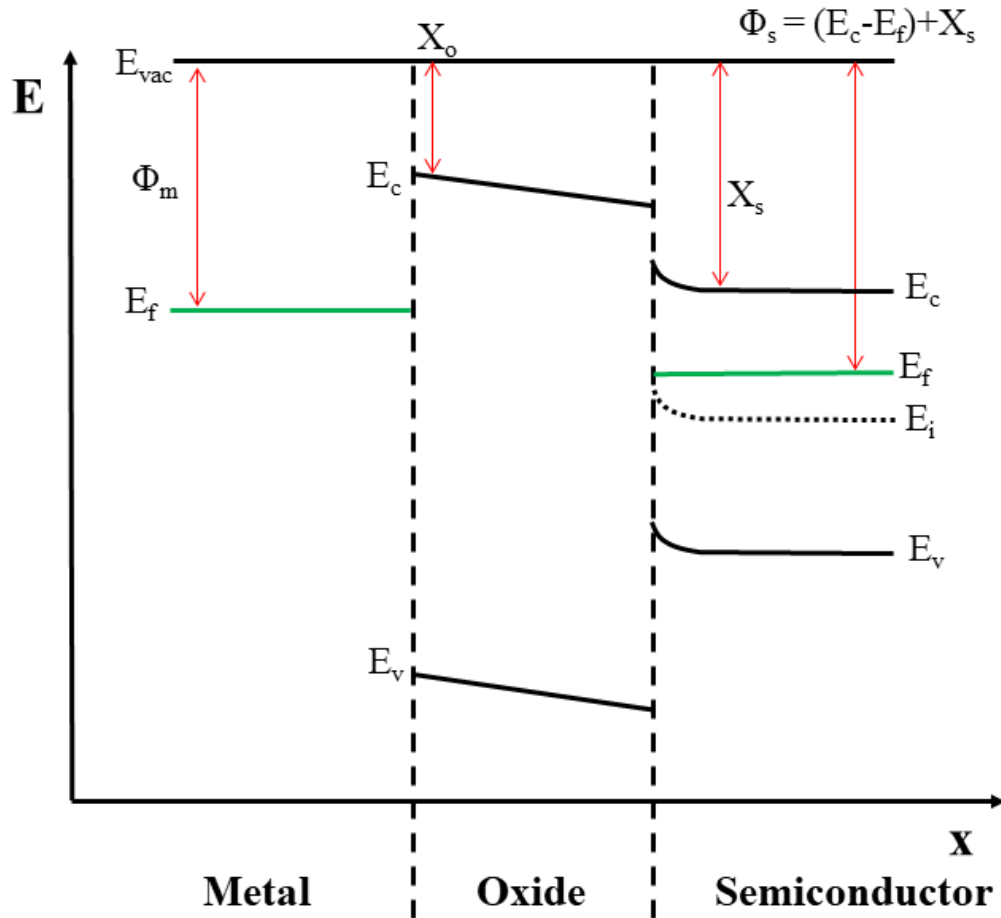


Figure 9: Depletion condition for a MOS stack. Symbols retain their previous meanings.

Eventually the MOS-stack will enter the inversion regime (see Figure 10). Here, minority carriers (holes) will be drawn up from the bulk of the semiconductor into what was previously the depletion region; now known as the inversion region. It is so called as it now contains mobile holes, so effectively this region of the semiconductor has become p-type (therefore inverted). Crucially it is this region which will respond to different measurement frequencies, as detailed below. This region also sees the intrinsic energy level of the semiconductor bend above the Fermi level; from a fundamental point of view

it is this crossover which determines that the DUT has passed into inversion. The point at which this crossover occurs is known as the threshold voltage, and this is also the maximum possible depth of the depletion region. The inversion region therefore appears as effectively flat on the C-V sweep as it no longer affects the total capacitance of the MOS-stack.

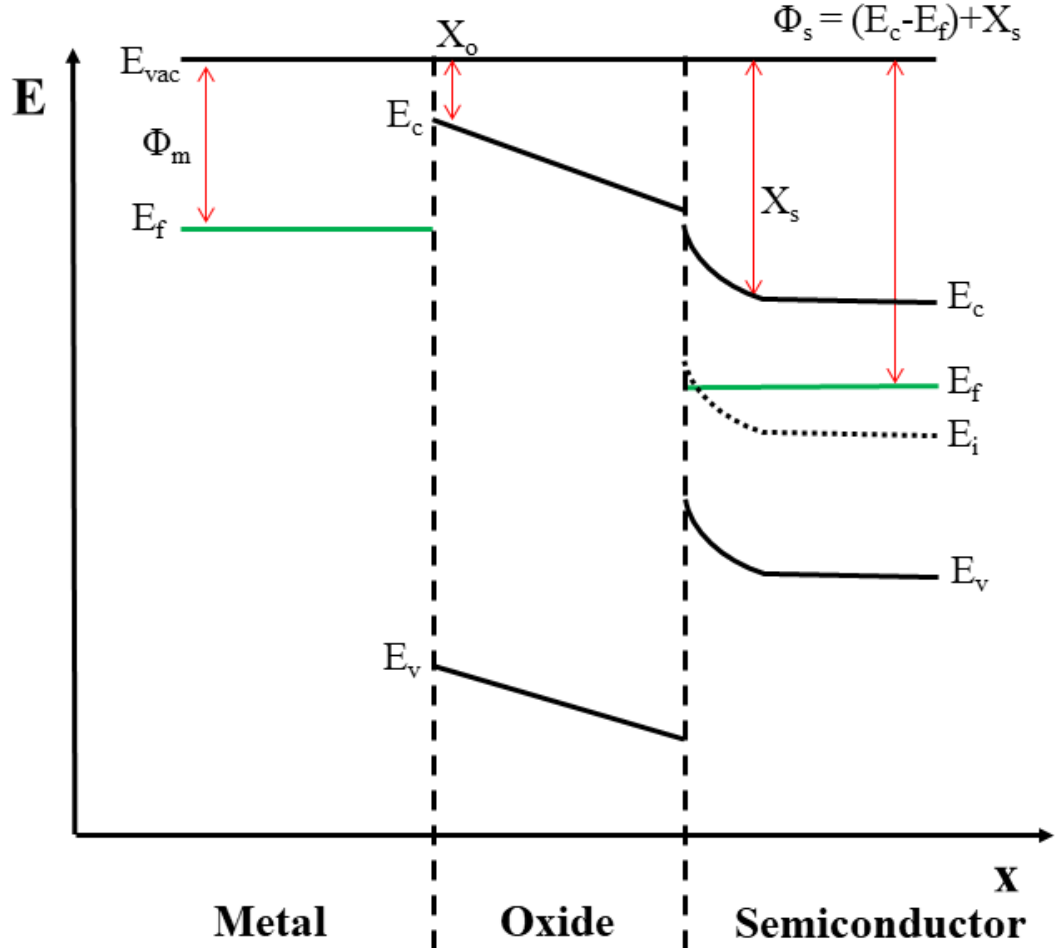


Figure 10: Inversion condition for a MOS stack. Symbols retain their previous meanings.

The inversion region will respond differently to varying AC measurement frequencies, and we can use this to our advantage to determine properties of the grown oxide. One such property of interest within this work is the interface state density D_{it} . Section 5 describes the techniques used. As a general rule, lower frequency measurement signals will cause an inversion response with a higher proportion of the total capacitance; the ideal being that a low-frequency signal shows an inversion response of exactly the same capacitance as seen in accumulation. Higher frequency signals will result in a lower measured capacitance as the carrier generation rate will be lower, due to the higher

frequency giving a smaller time frame in which carriers can respond to the applied voltage.

It is also important to note that as the DUT passes from accumulation into depletion, it passes through the flatband voltage V_{FB} ; this is shown in Figure 11. At this point there is no band bending (hence “flatband”). V_{FB} will vary for an individual semiconductor.

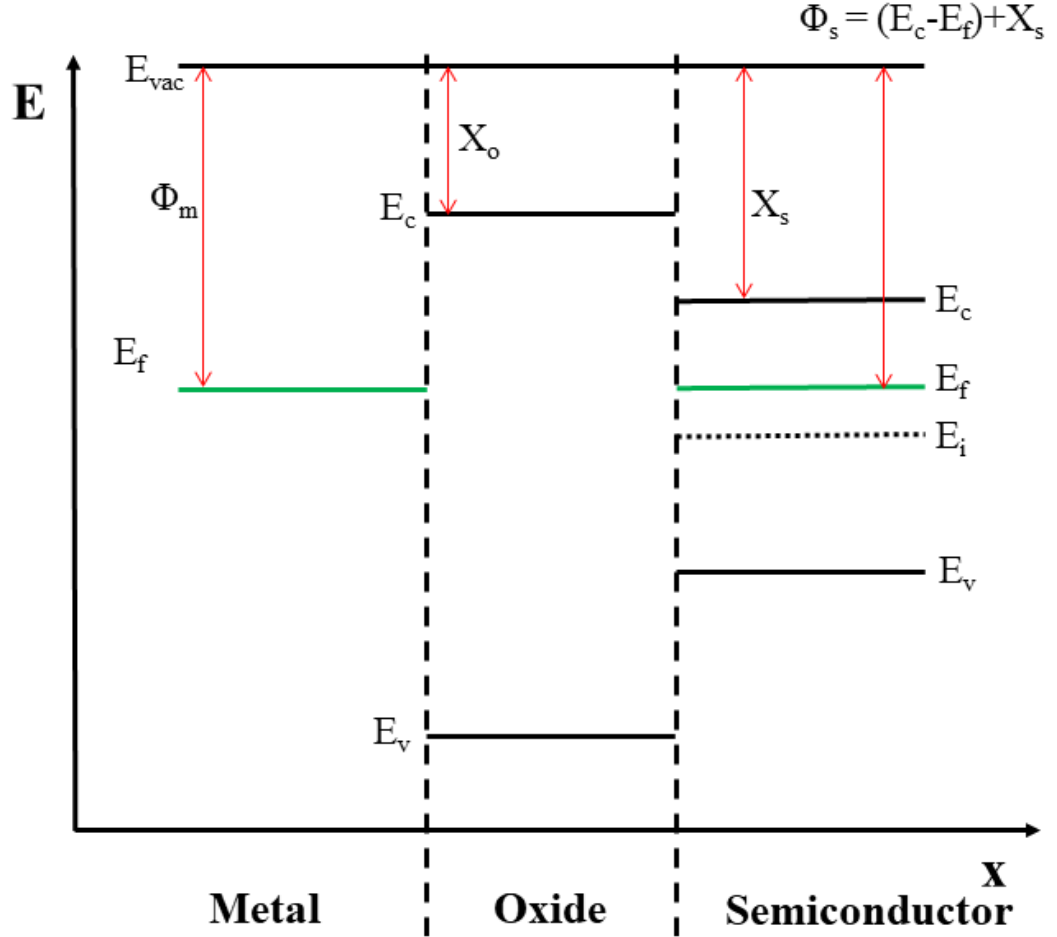


Figure 11: Flatband condition for a MOS stack. Symbols retain their previous meanings.

We can also consider the accumulation, depletion, and inversion regions with respect to their contributions to the total capacitance of the DUT. By considering the general definition of capacitance and the charge densities in different regions of the device, we can describe the total capacitance C as:

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_p + C_n + C_b + C_{it}}} = \frac{C_{ox}(C_p + C_n + C_b + C_{it})}{C_{ox} + C_p + C_n + C_b + C_{it}} \quad (23)$$

where C_{ox} is the capacitance of the oxide, C_p is the capacitance related to the hole charge density, C_n is the capacitance related to the electron charge density, C_b is the capacitance of the bulk material and C_{it} is the capacitance of any charges trapped at the interface. C_{ox} is in series with the other four capacitances, which are in parallel with one another. Figures 12-15 (reproduced without permission from ref. ¹⁵) show this diagrammatically.

In accumulation the electron charge density is high, hence C_p is also high; from equation (23) the dominant contribution is therefore C_{ox} and so we can determine the thickness of the oxide from these measurements using equation 26. Moving through to depletion, as the depletion region itself acts as a dielectric medium it contributes to the total capacitance as the bulk capacitance C_b ; there is also contribution from interface trapped charges, denoted by C_{it} . C_b and C_{it} are together in parallel, and in series with C_{ox} ; this causes a decrease in total capacitance. The contribution of C_{it} allows us to extract D_{it} in this regime.

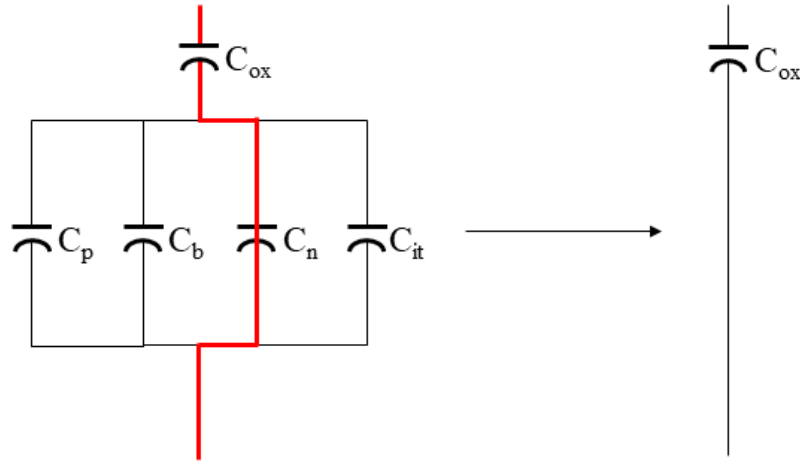


Figure 12: Capacitance diagram for accumulation condition. Only C_{ox} contributes. C_n is much larger than C_{ox} . C_p, C_b, C_n, C_{it} and C_{ox} are defined above.

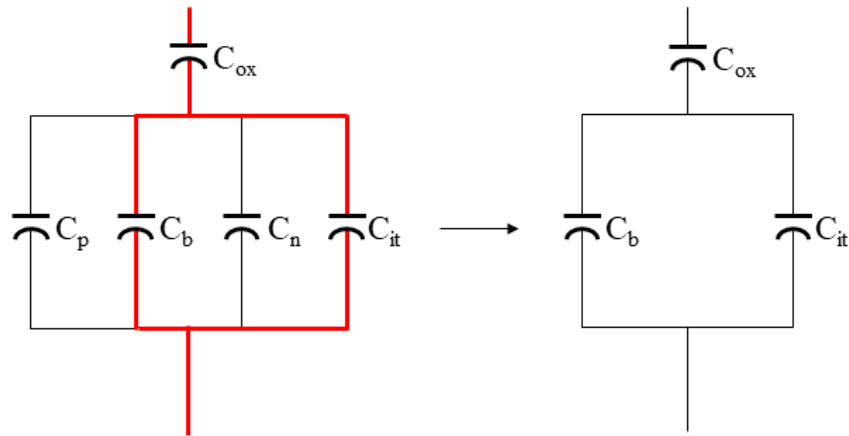


Figure 13: Capacitance diagram for depletion condition. Contribution from C_b and C_{it} lowers the total capacitance. C_{it} allows extraction of D_{it} in this regime.

In the inversion regime we see different behaviours for high- and low-frequency AC measurements. For sufficiently low-frequencies, the hole charge density C_p can follow the signal fully and only C_{ox} contributes. At higher frequencies C_p cannot fully follow the measurement signal, hence we see contribution from the bulk capacitance C_b . This is the maximum possible reduction in capacitance, so for the highest frequencies we observe the lowest total capacitance. The only instance in which we see lower total capacitance is if the DUT is driven into deep depletion. Deep depletion occurs when a high frequency measurement signal is applied whilst the gate voltage is swept sufficiently quickly that the MOS-stack is no longer in thermal equilibrium. This increases the thickness of the depletion region (hence “deep” depletion) as outside of thermal equilibrium the minority carrier generation rate is not sufficient to supply the amount of carriers required to form an inversion region. Therefore, as a thicker depletion region is formed, the total capacitance decreases.

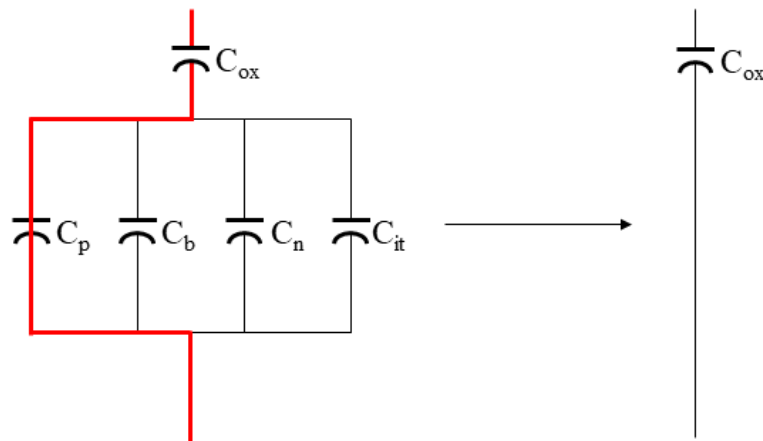


Figure 14: Capacitance diagram for low frequency inversion condition. Low frequency AC signal gives short circuit like in accumulation, so only C_{ox} contributes.

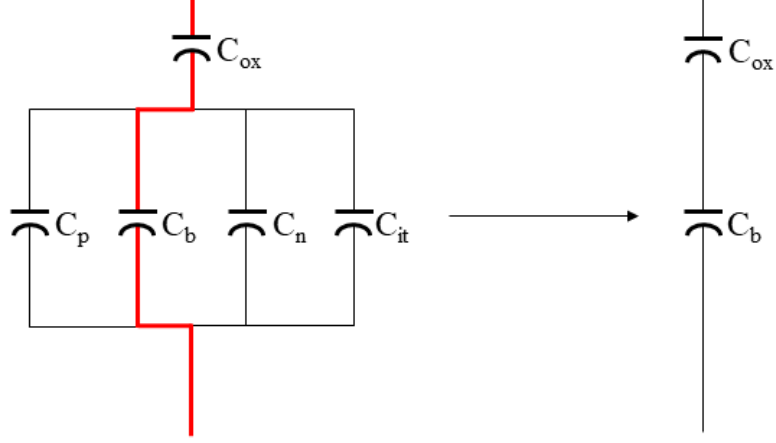


Figure 15: Capacitance diagram for high frequency inversion condition. High frequency AC gives contribution from bulk capacitance C_b , lowering total capacitance more than in other regimes.

2.3 Experimental methodology

For this research a high quality, fully relaxed 300 nm thick undoped 3C-SiC epilayer was grown on an on-axis p⁺ Si (001) substrate 150 mm in diameter. A 100 nm intrinsic silicon (i-Si) layer was grown on the substrate to improve the surface morphology of the substrate and to seal any defects present. The epitaxy was carried out in ASM Epsilon 2000 RP-CVD system^{39,40}, while all wafer handling, cleaving, and oxidation processes were performed in a ISO Class 5 cleanroom to minimise particulate contamination – see section 3.5 for further details. Particulate contamination can introduce device-killing issues including introducing charge trap sites into the oxide layer (hampering the electrical performance of the device) and can cause significant issues with the device fabrication process.

Samples of approximately 2×2 cm were cleaved from the grown epi wafers and dry oxidized in a conventional quartz tube furnace. All quartz components, including the boat in which the samples were placed, and the tools used to manipulate the samples within the quartz oxidation tube, were cleaned first with high-purity de-ionised (DI) water then with semiconductor-grade acetone. After rinsing with acetone, the same components were rinsed with semiconductor-grade isopropyl alcohol (IPA) to remove any residual acetone. As a final cleaning step, the quartzware was baked out in the tube furnace at a temperature of 350 °C for 15 minutes, under a constant flow of high-purity (9N) N₂. Samples were then introduced to the furnace under the same constant N₂ flow (approximately 5 slm), and the furnace ramped to 650 °C. At this point the gas flow was switched to ultra-high purity 6N (99.9999%) oxygen (O₂) at a flow rate of 1 slm. Dry oxidation was then

performed for between 1 and 10 hours at a temperature of 985 °C and a pressure of 1 ATM. Oxidation of material can be seen in Figure 16.

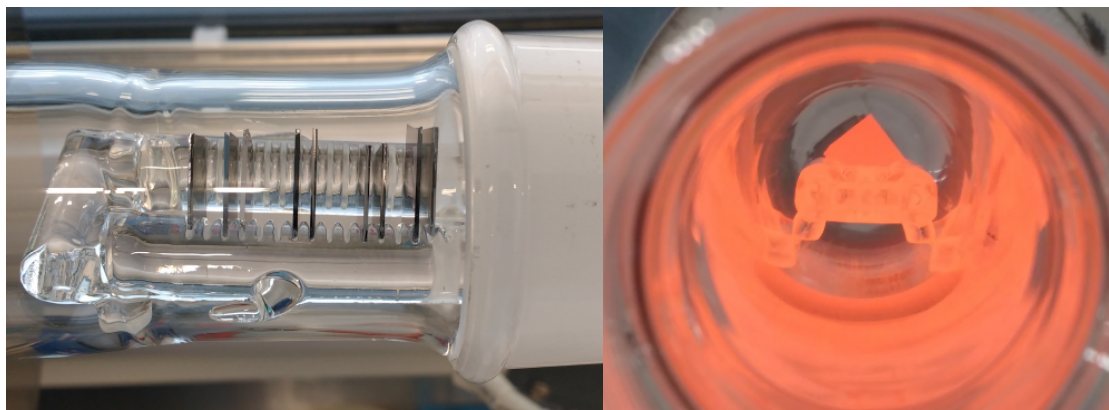


Figure 16: Oxidation of 3C-SiC in quartz tube furnace. 1.5×1.5 cm samples were loaded into the quartz oxidation boat (L) and oxidised at 985°C. (R) shows samples in the furnace at full temperature.

Several samples were oxidised at slightly higher temperatures (995 °C), however the tube furnace used in this work could not reliably maintain this temperature for the long oxidation times. As a result, the majority of the samples were oxidised at a stable 985 °C. Unless otherwise stated all samples referred to in this work were oxidised at this temperature. Care was also taken to ensure that the samples were all placed in the same area of the tube furnace as there was a temperature gradient across the tube. In practice the most reliable method for this was to oxidise each 2×2 cm sample individually. This is of course the least efficient use of O_2 , but in an industrial setting a large number of samples or entire wafers could be oxidised simultaneously in an industrial-scale oxidation furnace.

Once the oxide had been grown, a Panalytical X'Pert Pro MRD high resolution X-ray diffractometer was used to perform X-ray reflectance (XRR) measurements on all samples. X'Pert Reflectivity modelling software was used to ascertain the variance in oxide thickness with respect to oxidation time. This modelling software was adequate for thicker oxides (>10 nm), however it was not possible to model a precise thickness for thinner oxides (<10 nm). As such it was necessary to undertake cross-sectional transmission electron microscopy (X-TEM) analysis of the samples to accurately determine the oxide thicknesses.

Samples were prepared for X-TEM through a combination of mechanical polishing and argon milling. X-TEM analysis of the films was also used to qualitatively assess the crystallinity of the 3C-SiC epilayers, the quality of the oxide, and the interface between

the two materials. A JEOL 2100 TEM operating at 200kV was used to undertake all X-TEM analysis.

Atomic Force Microscopy (AFM) was used to measure the surface roughness of 3C-SiC epilayers and the grown oxide. X-ray photoelectron spectroscopy (XPS) and secondary-ion mass spectroscopy (SIMS) were also employed to analyse the composition of the oxide and check for contaminants. All of the material characterisation techniques used in this work are discussed in detail in section 4.

Electrical analysis was required to determine the behaviour of the carriers within the MOS-stack. To facilitate this, circular aluminium (Al) contacts 1mm in diameter and approximately 200 nm in thickness were deposited on the surface of the oxide by thermal evaporation in a vacuum of $\sim 1 \times 10^{-7}$ mbar. Deposition of contact materials for this and for the Hall-effect measurements are discussed in section 3.3. As with the oxidation process this evaporation was performed in ISO 5 cleanroom conditions and used high-purity (99.999%) Al source material. Samples were then mounted on Copper (Cu) plates using indium-gallium (InGa) eutectic paint. The Cu plate provided the back contact and all samples were isolated from the sample stages during electrical measurements using glass slides. Figure 17 shows a cross-sectional schematic of the entire MOS-stack.

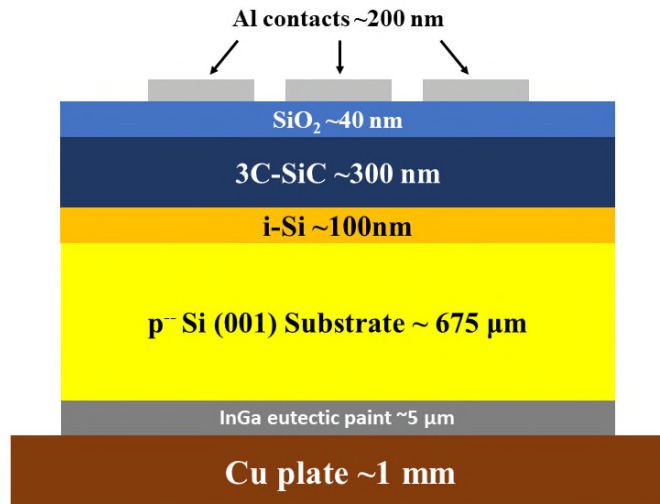


Figure 17: Cross-sectional diagram of MOS stack.

Capacitance-voltage (CV), conductance-voltage (GV), and current-voltage (IV) measurements were then taken for all samples, in electronically isolated probe stations which provided shielding from errant electric fields, and at room temperature. Probes were contacted to the Al contacts and the Cu plate, as can be seen in Figure 18. These probe stations were kept dark so as to avoid errant carrier generation from the Si substrate.

The i-Si layer was only found to significantly impact the electrical measurements at very low temperatures (see section 5.2.1).

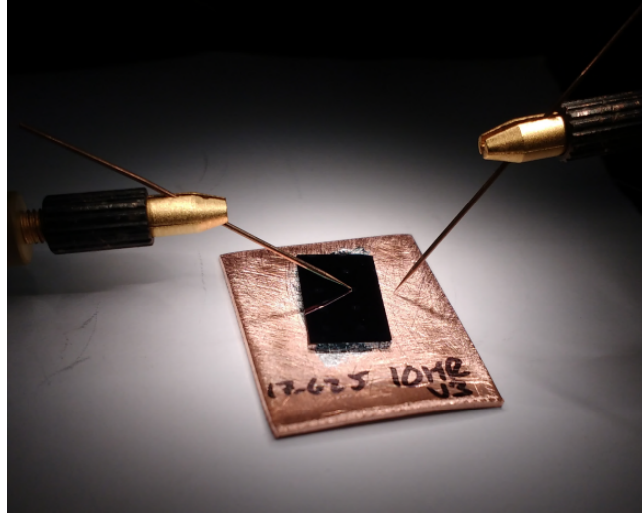


Figure 18: Electrical probes in contact with Al contact pad (L) and Cu plate (R). These measurements were taken in an electrically isolated dark box.

In addition, samples were cooled to a base temperature of approximately 80 K using a liquid nitrogen (LN₂) cooling system while CV and GV measurements were taken. An Agilent E4980A Precision LCR Meter was used for CV and GV measurements, while an Agilent 4156C Precision Semiconductor Parameter Analyser was used to take IV measurements.

For the CV and GV measurements an applied DC gate voltage was swept at a rate of 0.167 V/s, while a constant AC voltage of 25 mV oscillation was applied. A 5 s delay was applied before each sweep to allow for carrier redistribution. The current across the device is then measured, and from this the device capacitance C can be determined using equations 21 and 22:

$$C_s = \frac{I}{2\pi f V_{AC}} \quad (24)$$

$$C_p = \frac{C_s}{(1 + D^2)} \quad (25)$$

where C_s is the series device capacitance, C_p is the parallel device capacitance, I is the DUT current, f is the AC signal frequency, V_{AC} is the applied AC voltage RMS magnitude and phase angle, X is the reactance, and D is the dissipation factor (i.e. leakage).

Similarly, the conductance G can be determined using equation 23:

$$G_p = \frac{R_s}{(R_s^2 + X_s^2)} \quad (26)$$

where G_p is the parallel conductance and R_s is the series resistance.

In practice, C_p and G_p are calculated by the LCR meter. For most MOS device applications the parallel capacitance and parallel conductance are the parameters of interest, and all references herein to capacitance and conductance refer to these values.

Varying the frequency of the applied AC bias will change the response of the carriers and hence the measured capacitance. The higher the frequency of the applied AC signal, the quicker this signal “flips” from positive to negative bias (as the AC signal is sinusoidal), and hence the shorter the time the carrier have to respond to this signal. This effectively means that the capacitance is larger for lower frequencies as more carrier build-up at the metal/oxide and oxide/semiconductor interfaces can occur. In this work a range of AC bias frequencies between 100 Hz and 1 MHz were swept. As discussed below, frequencies up to around 10 kHz were deemed valid for the 3C-SiC MOS devices, with higher frequencies not providing an accurate measure of carrier behaviour – see section 5.2.1.

3 Device fabrication

3.1 Introduction

Device fabrication is an intrinsic part of all modern semiconductor physics, for both cutting-edge research and everyday component production. Over the past 60 years or so a vast array of techniques have been developed, allowing physicists and engineers to create bespoke devices for an almost unlimited number of end uses. While only a fraction of the techniques that are used every day in device manufacture have been used within this research, those listed herein are commonplace within the semiconductor industry at large. The equipment available at the University of Warwick is of course more suited to prototyping and small-scale research than large-scale production, but the principle of operation is very similar.

The photolithography equipment, for example, uses the contact-mask method. The reality for large-scale device manufacture is that the devices are so small that contact-mask

photolithography does not have sufficient resolution to create these devices. The techniques used to achieve such small device sizes are slightly different – for example using extreme ultraviolet light (EUV) rather than UV to expose the photoresist, but the basic idea of curing a photoactive resist to create a shape is the same⁵². As such the techniques described in this work are sufficiently similar to industrial techniques to assume that any adaptations required are simple and can use existing industrial technology. The 3C-SiC epilayers have been grown on Si substrates specifically to allow for existing semiconductor device fabrication technology to be used in device production; homoepitaxial 3C-SiC is much more expensive, which is a barrier to market entry. It is also only available in much smaller wafer sizes⁵³. 3C-SiC is also around 1.5 times more dense than Si (3.21 gcm^{-3} compared to 2.32 gcm^{-3} ^{28,54} meaning that 3C-SiC substrates are much heavier.

The devices discussed in this work have been fabricated to determine the material properties of both 3C-SiC and oxides grown thereon at low temperatures ($<1000 \text{ }^{\circ}\text{C}$), not as prototypes of devices for specific power electronics functions. This fact notwithstanding, it was important to analyse the potential for fabrication of more complex devices (such as MOSFETs) which may have more specific applications^{18,55,56}. In this way, this work lays a foundation for further research with greater application.

3.2 Photolithography

Contact-mask photolithography is the process by which most of the device structures described in this work have been produced, both to define metal contact areas and Hall bar mesas. This process relies on the UV sensitivity of some photoactive compound (PAC) in a solution, known as a photoresist (hereafter also ‘resist’). In this work, the two photoresists used were Merck AZ 5214 E and Microposit S1813 (hereafter ‘AZ’ and ‘S18’ respectively). The PAC in both of these resists is diazonaphthoquinone (‘DNQ’)^{57,58}. Incident UV light changes the solubility of DNQ, and then heating the sample to different temperatures will change the properties of the photoresist as required by the specific process (as detailed below).

Choice of photoresist is dependent on the desired resist side wall profile for the device in question. For a comprehensive review of photolithography, see C. Macks’ *Fundamental Principles of Optical Lithography*.⁵⁹ All possible sidewall morphology is a complex

subject and is outside the scope of this thesis, but for most photolithography at the scales discussed here it is sufficient to consider simply whether the profile is positive or negative. While many other parameters can also affect side wall profile, in general the choice of either a positive or negative photoresist will result in the profiles as seen in Figure 19. Resists are termed positive or negative based on the image produced; in a positive resist the areas exposed to UV remain, and vice versa for a negative resist. This is what forms the slope of the side walls – the incident UV will diffract as it passes through the resist layer, spreading laterally. This forms an exposed area which is broader at the substrate than at the resist surface. When the unexposed regions are then dissolved (see below) it leaves the resist with side walls sloping either downwards (positive resist) or upwards (negative resist), as Figure 19 shows.

In this work negative resist (AZ) was used for almost all metal deposition as the undercut profile makes for better metal lift-off. Positive resist (S18) was used for mesa definition. This is principally because a positive resist will result in a resist image the same as that on the contact mask; this makes alignment of mesas (for Hall bars, for example) much easier.

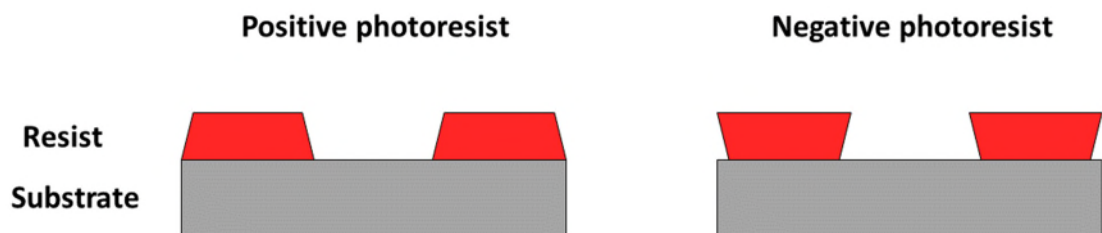


Figure 19: Side wall profiles for positive and negative photoresists. Side wall angle has been exaggerated for clarity.

The lithography process is slightly different for positive and negative resists.

Figure 21: Pre-exposure bake of resist. Resist is spun on to a thickness of 1.2-1.6 μm and baked at 110 $^{\circ}\text{C}$ to remove approximately 60% of the solvent by weight.

Figure 22: Contact-mask exposure to define windows in resist. In reality the mask is in direct contact with the resist surface; here it is separated to show the windows.

Figures 21-32 show the main steps used in this research to fabricate a Hall bar by photolithography, which involves both positive and negative resist processes. The contact mask used to define the windows determined the size and dimensions of the Hall bars. The same contact mask was used for all Hall bars; Figure 20 shows the dimensions.

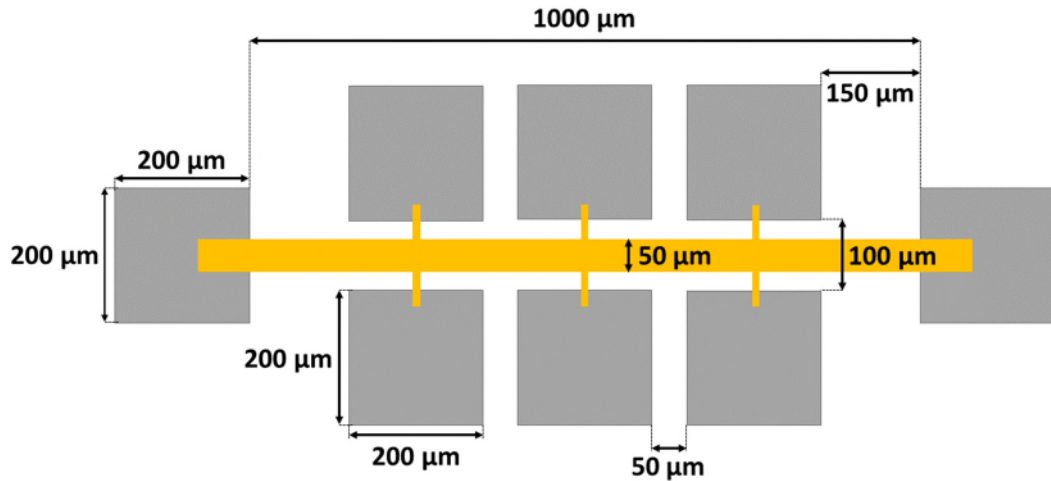


Figure 20: Layout diagram for Hall bars showing key dimensions.

The first step with either process is to apply the photoresist in a thin, even layer. The example below describes the process for fabricating a Hall bar, which is a device that exploits the Hall effect to examine the carrier behaviour in the epilayer; see section 5.3. The first step for fabricating a Hall Bar uses a negative photoresist – in this case AZ. Typically the resist is dropped or sprayed on the sample surface and then spun to the desired thickness. Controlling thickness is key for both the UV exposure and metal deposition, and a balance must be struck between keeping the resist sufficiently thin that the UV exposure is even throughout the resist, and sufficiently thick that any deposited metal will break cleanly during lift-off, creating a sharp edge for any contacts deposited. Optimal thickness of AZ and S18 resist tends to be 1.2 - 2.0 μm . Resist thickness was varied as part of the effort to optimise the device fabrication process, and the optimal thickness was found to be around 1.6 μm .

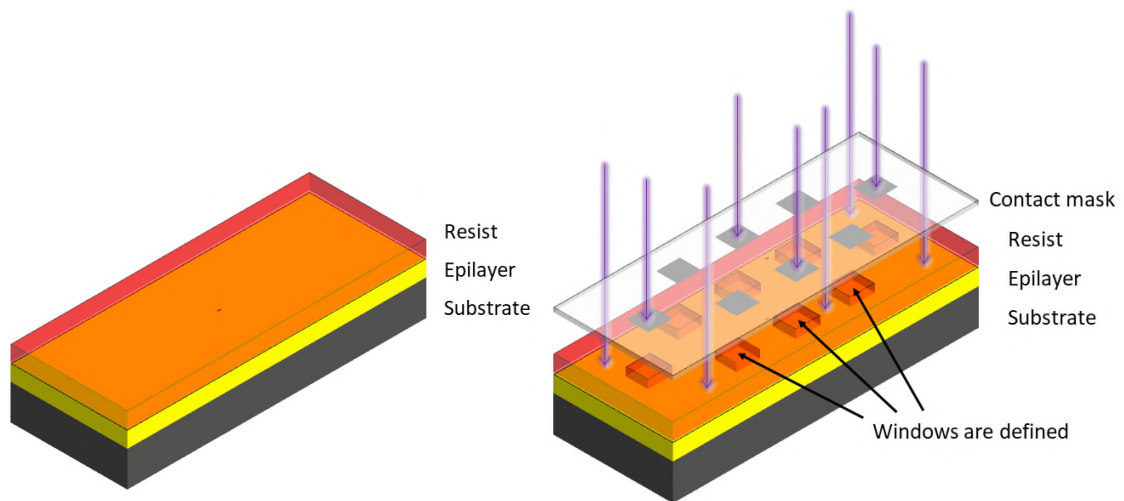


Figure 21: Pre-exposure bake of resist. Resist is spun on to a thickness of 1.2-1.6 μm and baked at 110 $^{\circ}\text{C}$ to remove approximately 60% of the solvent by weight.

Figure 22: Contact-mask exposure to define windows in resist. In reality the mask is in direct contact with the resist surface; here it is separated to show the windows.

Following spinning the resist is given a pre-exposure bake

Figure 21: Pre-exposure bake of resist. Resist is spun on to a thickness of 1.2-1.6 μm and baked at 110 $^{\circ}\text{C}$ to remove approximately 60% of the solvent by weight.

Figure 22: Contact-mask exposure to define windows in resist. In reality the mask is in direct contact with the resist surface; here it is separated to show the windows.

; this evaporates some of the solvent in the liquid resist to make it more stable and adhere to the epilayer. A mask that is in direct contact with the sample can then be used without stripping the resist. Care must be taken at this stage to ensure that only the solvent evaporates and no crosslinking occurs; close temperature control (to within 1 $^{\circ}\text{C}$) is sufficient to do so.

Exposure to UV light (Figure 22) will cause the DNQ to photolyse to a ketene, which then reacts with water present in the photoresist to form indene carboxylic acid. This initial exposure is performed with the contact mask in place, and it is this stage which defines the device structure. The sample then undergoes a reverse bake, which is at a higher temperature than the initial pre-exposure bake (Figure 23

Figure 23: Post-exposure bake. Here unexposed resist is crosslinked, permanently defining the contact windows

Figure 24: Flood exposure. All remaining photoresist is photolyzed.

). The higher temperature is enough to activate the crosslinking compound within the resist, which reacts with the exposed resist to become extremely resistant to the developer (typically dilute tetramethyl ammonium hydroxide, TMAH). This is one of the most vital steps of the photolithography process, as it is this which will determine the resolution of

the resist pattern. Too high a temperature will begin to crosslink the unexposed resist, while too low a temperature will not sufficiently crosslink the resist; either will result in distortion of the desired pattern. The same can happen with over- or under-exposure of the sample during the contact-mask exposure stage.

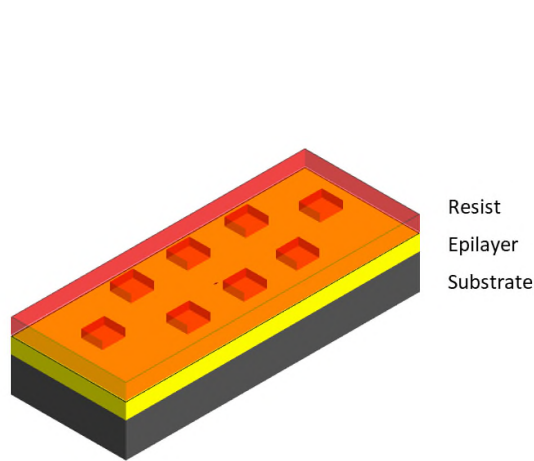


Figure 23: Post-exposure bake. Here unexposed resist is crosslinked, permanently defining the contact windows

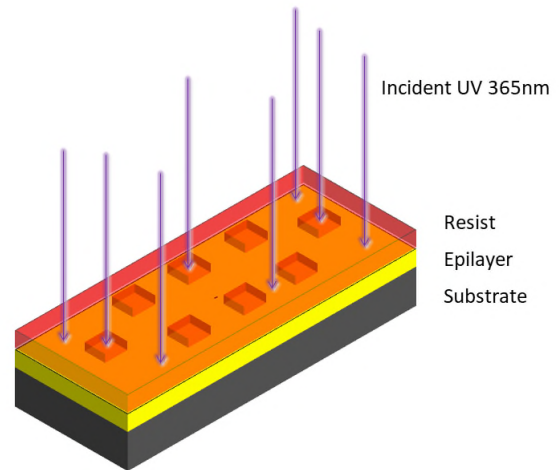


Figure 24: Flood exposure. All remaining photoresist is photolyzed.

A flood exposure (Figure 24), whereby the entire sample surface is exposed to UV with no mask in place, is the next step. This exposure is generally much longer than the initial contact-mask exposure and photolyses the DNQ in the remaining resist- i.e. that which was not previously exposed. The crosslinking compound prevents the DNQ in previously exposed areas from photolysing. This results in areas under the original contact mask (known as windows) being extremely soluble in the developer, while everything else is resistant to the developer. Thus, when the sample is developed, the contact mask pattern is present as windows in the resist (Figure 25). From here, further processes such as metal deposition can be applied. Figure 26 shows the sample with metal deposited across the entire surface; dissolving the remaining resist in a suitable solvent (typically isopropyl alcohol (IPA) or acetone) will leave the metal only on the desired contact pad areas, i.e. the windows opened in the resist (Figure 27). Many different techniques can be employed for metal deposition, which are explored in detail in Section 3.3.

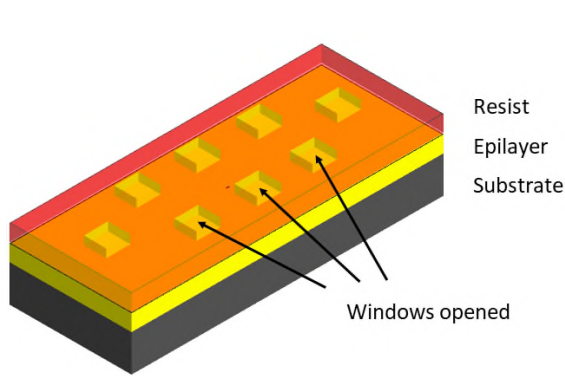


Figure 25: Development of resist. Areas blocked by the contact mask during the initial exposure dissolve in the developer, leaving open windows ready for metal deposition.

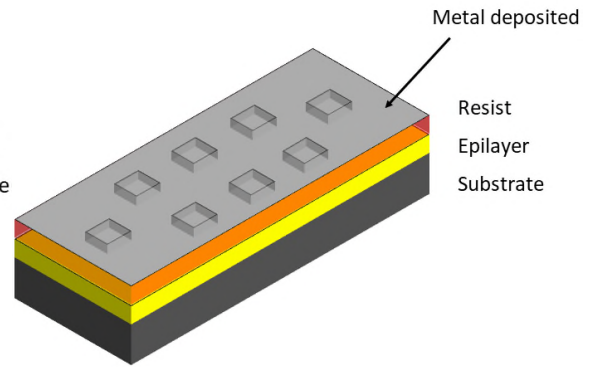


Figure 26: Metal deposition across entire sample surface. Several different methods can be employed to deposit the metal, as described in Section 2.3.

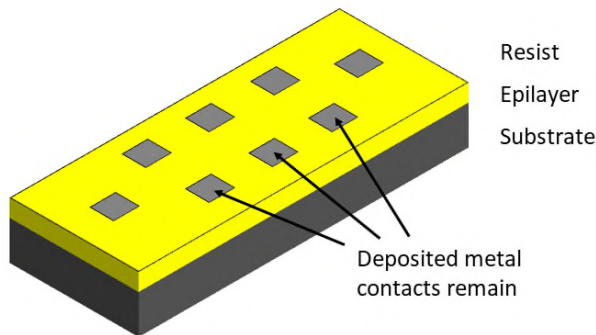


Figure 27: Resist is dissolved in suitable solvent (typically acetone or IPA) to leave only the metal contacts. Optimising resist thickness at the start of the fabrication process ensures well-defined contacts.

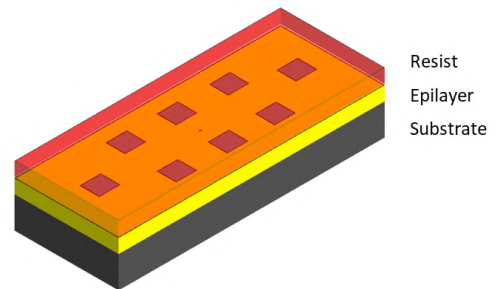


Figure 28: Second spin and pre-exposure bake. Resist thickness is less critical for mesa steps as for metal deposition, but side wall profiles must be considered, particularly for very narrow mesa structures.

Once contact pads have been fabricated, the Hall bar mesa can be etched from the epilayer. This process is similar to defining the contact pad areas but is a positive photoresist process rather than a negative one. As such the process is somewhat simpler. As before the first step is to spin and bake on a thin, even layer of photoresist (Figure 28) and expose this resist to UV light, selectively blocking the desired mesa area with the contact mask (Figure 29

Figure 29: Contact-mask exposure defining the mesa. Correct alignment of the mask is crucial. Again for the purposes of this diagram the mask is shown at a height above the resist surface but in reality must be in contact.

Figure 30: Mesa defined in remaining photoresist. Definition of the resist with determine the success or failure of the RIE.

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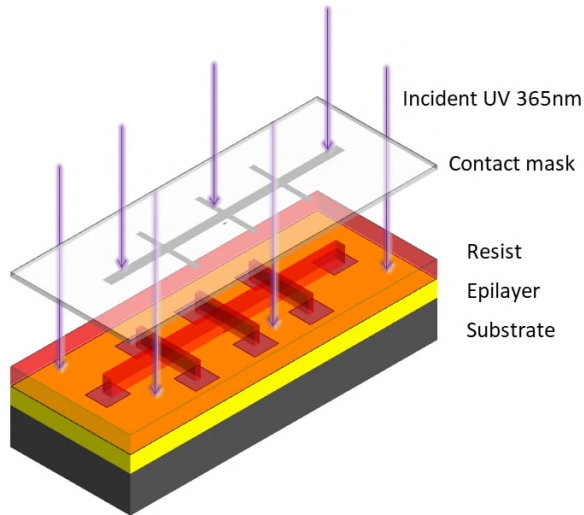


Figure 29: Contact-mask exposure defining the mesa. Correct alignment of the mask is crucial. Again for the purposes of this diagram the mask is shown at a height above the resist surface but in reality must be in contact.

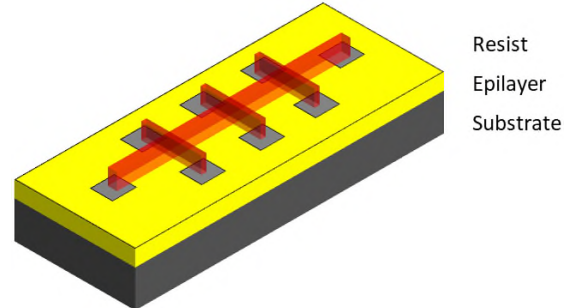


Figure 30: Mesa defined in remaining photoresist. Definition of the resist with determine the success or failure of the RIE.

The UV-exposed areas are much more soluble in the developer (again dilute TMAH), and so when the sample is developed only the area defined by the contact mask remains (Figure 30). At this stage great care must be taken to ensure that the mesa aligns correctly with the contact pads as the calculation of key parameters such as mobility and Hall coefficient (see Section 5.3) is dependent on the arrangement and spacing of contacts. It is also vitally important to align correctly to crystallographic planes for fabrication of any suspended structures, as wet etchants typically used (such as TMAH) are anisotropic and will preferentially etch the (111) plane. Although it can be argued that the orientation of any devices is somewhat arbitrary if said devices are not to be suspended, in practice it is often useful to use the crystallographic planes to orient the sample when depositing contacts and defining mesas. As such all Hall bars fabricated as part of this research were aligned to the (100) or (010) planes. The design of the contact mask included identical Hall bars at 45° to the (100)- and (001)-oriented Hall bars, so these were aligned to the (111) plane. The (111)-oriented Hall bars were most suitable for suspended devices as TMAH preferentially etches Si along the (111) plane⁶⁰.

Once the mesa shape had been defined in photoresist atop the epilayer, a reactive-ion etch (RIE) (Figure 31) was used to etch away the 3C-SiC epilayer in all other areas, leaving only the mesa. RIE uses a high-energy plasma of a specific reactive ion to only etch the epilayer. In this research sulphur hexafluoride (SF_6) was used exclusively. The process is

described in more detail in section 3.4. The remaining resist was then dissolved away to leave only the epilayer mesa (Figure 32). This device is then ready to chip packaged and electrical measurements taken; however, in practice it was necessary to employ some thermal annealing processes to ensure that the contacts deposited were ohmic. This is explored in Section 3.3.5 below.

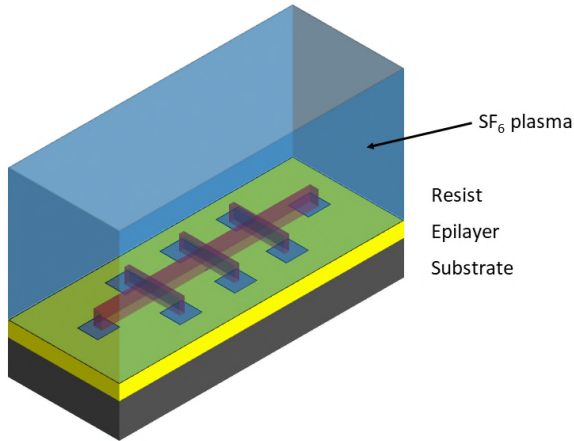


Figure 31: Reactive Ion Etch (RIE) of sample. Areas covered by resist and by metal contacts will not be etched. For this research SF₆ was exclusively used for RIE.

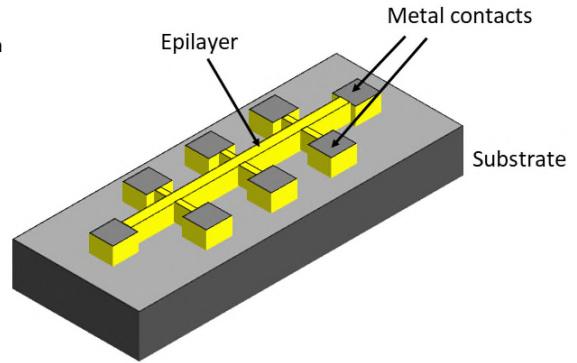


Figure 32: Final device after RIE etching. contact annealing is mostly commonly performed at this stage to ensure that metal contacts are ohmic.

3.3 Metal contacts

3.3.1 Ohmic behaviour

For the devices fabricated as part of this research it was important that the interface between the metal contact and the 3C-SiC showed ohmic behaviour. Typically this is discussed in terms of the contacts themselves being ‘ohmic’ (i.e. has a linear voltage-current curve, obeying Ohm’s law), although it is important to remember that for any such reference we are in fact referring to the interface between the metal and the semiconductor, not just the contact metal itself. A low resistivity (on the order of $1 \times 10^{-5} \Omega\text{cm}^2$) is also preferable – both as any additional device resistance will contribute to any resistivity measurements of the 3C-SiC itself, increasing error, and as non-ohmic behaviour of contacts will impede collection of accurate data on other device or epilayer parameters. It is also vital to ensure that the metal-semiconductor barrier is non-rectifying; i.e. that the contacts behave the same (and are ohmic) whether a positive or negative bias is applied. All analogue electronics use AC signals, so if contacts are rectifying half of

the signal would effectively be blocked, rendering the device worthless for any analogue application.

Choice of contact material is key here, and much literature has been written on the most suitable semiconductor-metal interfaces for a wide variety of semiconductors at various levels of doping. For SiC, Porter and Davis present a comprehensive review of commonly used contact metals for a number of polytypes, including both p- and n-type 3C-SiC ⁶¹. For p-type 3C-SiC, all but one contact metals discussed include Al. Al is very common as a contact material for p-type SiC as it is itself often used as a p-type dopant. Deposition and annealing of an Al contact can therefore create a very highly doped region at the surface of the SiC, which allows carriers to tunnel easily across the interface. Thermally evaporated Al was reported to have a contact resistivity of $3.1 \times 10^{-2} \Omega\text{cm}^2$ after a 3 minute, 880 °C anneal ⁶². The combination of this relatively low contact resistance and the ready availability of the equipment needed to thermally evaporate Al led to the decision to use Al as a contact material for all the p-type 3C-SiC studied as part of this research. Sputtering of Al was also explored as a quicker deposition method – see section 3.3.2.

Ni is a common contact material for n-type SiC ⁶¹. Wan et al. found that Ni could provide a low resistivity ($5 \times 10^{-5} \Omega\text{cm}^2$) contact for 3C-SiC following thermal annealing at 700 °C, and that this resistivity further decreased with increasing anneal temperature. It was demonstrated that with anneals of 1000 °C contact resistivity could be reduced to values as low as $1.4 \times 10^{-5} \Omega\text{cm}^2$ ⁶³. It is important to note that this resistivity value is three orders of magnitude smaller than a “low” resistivity value for contacts formed on p-type 3C-SiC. Porter and Davis report that the defect density of the 3C-SiC may contribute significantly to the contact resistivity ⁶¹, and as in many cases the defect density of the 3C-SiC was not reported it is not always possible to directly compare with that grown for this work.

Ni is a silicide former, which may contribute to the ohmic behaviour of the contacts in ideal conditions ^{64,65}. It also oxidises readily, and so for this project a NiCr alloy was used for contacts on n-type 3C-SiC. This alloy is significantly less prone to oxidation than pure Ni, and has the added bonus that Cr is a carbide former. As such the NiCr contacts typically had very good adhesion and did not suffer the lift-off issues that were encountered with Al (see section 3.3.3). They did however appear to oxidise extremely

readily when exposed to the high temperatures encountered during thermal annealing, as discussed below. This was a major inhibiting factor in fabricating functional devices.

Another consideration when laying electrical contacts is the influence of the Schottky barrier height and of Fermi level pinning. This phenomenon is observed to different degrees in many semiconductors, including SiC ⁶⁶. The Schottky-Mott model ^{3,67} posits that as a metal and a semiconductor are brought together, the bands in the semiconductor will bend such that their work functions match. The Schottky barrier height can therefore be approximated as:

$$\Phi_B \approx \Phi_{metal} - \chi_{semiconductor} \quad (27)$$

However, this approximation was found experimentally to be inaccurate. Fermi level pinning, a phenomenon in which the bandgap is locked or “pinned” to the Fermi level of the semiconductor, can dominate the barrier height such that the contribution of the metal is effectively nil and it is defined solely in terms of the band gap of the semiconductor. Bardeen attributed this to the surface states of the semiconductor, explaining that if the density of these states is sufficiently high (larger than approximately $1 \times 10^{12} \text{ cm}^{-2}$) then the space charge layer at the metal/semiconductor interface is independent of the metal ⁶⁸. The Schottky barrier is therefore also independent of the metal.

Hara et al. demonstrated control over Schottky barrier heights and unpinning of Fermi levels by controlling the density of electronic states at the metal/semiconductor interface ⁶⁹. In this work thermal annealing was the method by which this was controlled. Interface state density of the metal/3C-SiC interface was not measured directly as for the purposes of this initial research it was sufficient for contacts simply to be ohmic. CV measurements were used to assess the interface state density of grown oxides (see section 5.2); a similar technique could be employed here for the metal contacts.

3.3.2 Sputtering

Sputtering is a very common method for depositing metal on semiconductor surfaces, as many non-magnetic metallic elements or compounds can be used ⁷⁰. It can be achieved through a variety of means, but all share the same basic principle; sufficiently exciting the surface of a target material by bombarding it with a plasma of high-energy ions such that it enters a gas phase, and then condenses onto the desired material. For all of this

research a conventional argon-ion (Ar^+) magnetron sputterer system was used. Similar equipment is widely used within the semiconductor industry to deposit thin films onto all manner of substrates. Figure 33 is a diagram of the sputtering setup used.

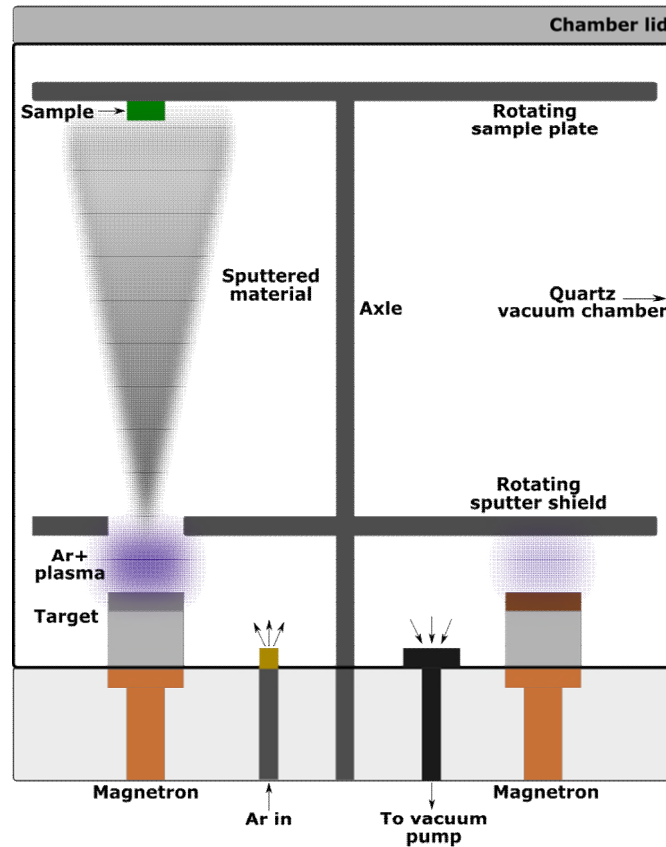


Figure 33: Sputtering Al with an Ar plasma. Sputtering is assumed to be cone-like projecting from the target surface. Rotating shields were used to ensure only the intended target metal was deposited onto the sample.

As the name implies, the Ar^+ magnetron sputterer employs magnetron sputter guns to generate a plasma and confine it close to the surface of the sputter target through use of a strong magnetic field. This field confines the ions to helical paths around the magnetic field lines, hence keeping the plasma within the boundaries of the sputter target (which is typically of a similar diameter to the magnetron gun). The system works at a reduced pressure, having been pumped down to 1×10^{-5} mbar and then backfilled with Ar to 1×10^{-3} mbar. This is vital as the separation of the substrate and the source target is fairly large (approximately 30 cm). At this reduced pressure, the mean free path of any sputtered material on the order of around 10 cm – not long enough that the material can reach the intended deposition areas. The Ar present in the chamber acts as a moderator, meaning that the sputtered material diffuses through this gas and condenses onto the sample. One downside to this approach is that the material also condenses on the walls of the chamber

and on the sample plate; however shielding can mitigate this to some extent. Isolating the plasma to an individual target also minimises cross-contamination of different sources in a multi-target setup such as that used in this research. A rotating shield was also used to minimise cross- contamination; whenever a plasma was generated above the target, the other two targets were covered by a metal sheet a few centimetres from the target surface. This meant that even if a plasma was generated above all three targets, only material from the chosen target could reach the sample.

Sputtering is a relatively quick process, with each deposition in this work typically taking less than an hour, including pump time. As such it was very useful for quick prototyping and fine-tuning parameters in the photolithography process, particularly the photoresist thickness. As the sputter rate is dependent on the plasma energy, which in turn is dependent on the electrical input power to the magnetron gun, by varying the sputter time with a constant input energy a specific thin film deposition thickness was possible to an accuracy of around 10 nm. It was therefore an easy task to consistently deposit thin films of desired thickness. In this work the typical contact thickness was around 200 nm, which allowed sufficient thickness for a good quality ohmic contact to be formed after annealing while not being so thick as to introduce issues with lift-off during the lithography process.

While sputtering is a useful technique to quickly deposit material, compared to other methods it introduces a much larger amount of contamination. The main source of this contamination is that the process operates at substantially higher pressure than, for example, thermal evaporation (see section 3.3.3); using deposition pressures of 10^{-3} mbar compared to 10^{-6} mbar. The sputtering system is purged of air to a pressure of around 10^{-5} bar and then back filled to 10^{-3} mbar with Ar, but this process still introduces more opportunity for contamination than operating at lower pressure. Oxidation was a consistent problem with sputtered Al, as can be seen in Figure 34. The poor quality of sputtered Al contacts both prevented wires being bonded to the samples when they were packaged into chips for analysis and gave poor adhesion of the Al to the material onto which it was sputtered. As such thermal evaporation was the preferred method for sputtering Al contacts for all p-type 3C-SiC samples and all undoped 3C-SiC MOS stack samples. Sputtered NiCr did not suffer the same oxidation issues during metal deposition, and so was the contact material of choice for all n-type 3C-SiC devices. Figure 34 (R) shows some of the high-quality contact pads made by sputtering NiCr.

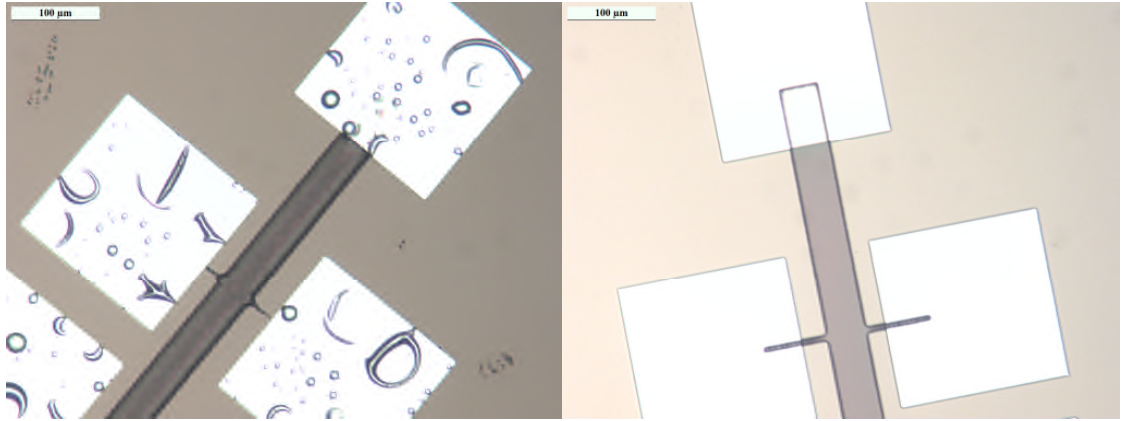


Figure 34: Sputtered Al contacts (L) and sputtered NiCr contacts (R). Note the buckled and oxidised areas on the Al indicating the poor contact quality compared to the smooth and clean NiCr.

Another disadvantage to sputtering for metal deposition is that the sputtered material is displaced from the target by way of an accelerating voltage. While the impact of this was not explored within the scope of this project, the literature suggests that this will lead to metal ion implantation within the substrate material ^{71,72}. While this was not considered a problem when depositing metal onto 3C-SiC epilayers for use as contact pads, for MOS stacks this was a major consideration. Implanted ions could theoretically act as fixed charge traps, impinging the operation of the MOS device ¹⁵. Thermal evaporation was therefore used to deposit all MOS-stack contact pads.

3.3.3 Thermal evaporation

Thermal evaporation is a very straightforward technique that involves placing the deposition material (e.g. Al or Au) in a very high vacuum (5×10^{-8} mbar) and heating it with a filament under high current such that it melts and then evaporates. It will then condense on any available surface, so a substrate or epilayer inside the chamber will experience the metal deposition. The profile through which the evaporated material spreads will vary with the type of filament used. In this work different filaments were used for different materials; a tungsten (W) coil was used to evaporate Al, while an alumina (Al_2O_3) basket was used for Au evaporation. These would give a point-like or cone-like evaporation profile respectively, as can be seen in Figure 35.

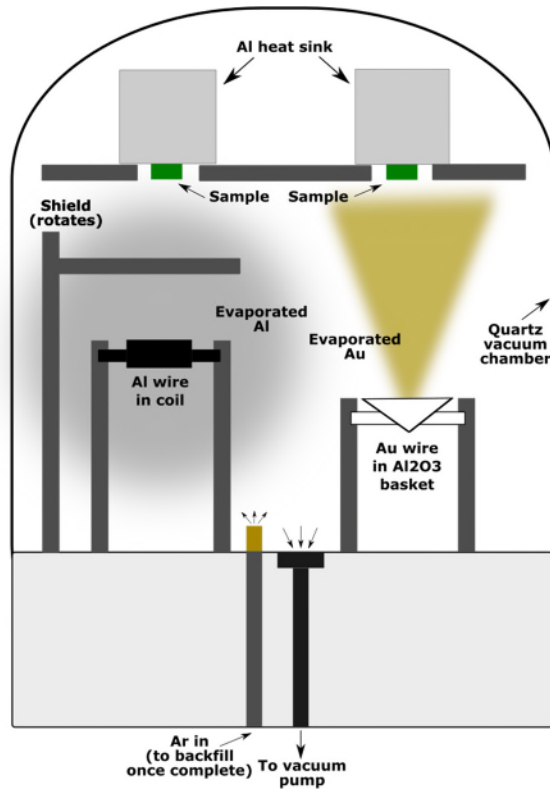


Figure 35: Diagram showing Al and Au evaporation conditions side by side. Note that evaporation of the Al is assumed to be point-like and the Au to be cone-like due to the design of the evaporation filaments.

The great benefit to thermal evaporation is that the high vacuum conditions ($\sim 10^{-6}$ mbar) give a very clean environment in which the metal will evaporate, meaning that the resultant contacts are very pure metal. As with any metal deposition process, the initial evaporation will be of native oxides formed on the surface of the deposition material. A shield was therefore used to protect the substrate material from the evaporated material for several seconds as the evaporation began. This resulted in high quality contacts with little to no oxide apparent.

The other great advantage to thermal evaporation is that the process is simply driven by thermal energy – there is no accelerating voltage. As such the energy of the evaporated material is much lower than a process such as sputtering, so there is much lower risk than metal will become embedded into the substrate. This made evaporation the ideal method for depositing MOS-stack capacitance dots (see section 3.3.3). Both Au and Al were explored as potential contact materials, but it was found that adhesion was relatively poor for Au dots and so the dots themselves were often irregularly shaped. This made estimating oxide thickness using capacitance measurements prone to a large error (see section 5.2.1). Al was found to have much better adhesion quality and hence could produce much more consistent, round capacitance dots.

One limitation of thermal evaporation is that the high vacuum necessitates a long pump time, which limits its usefulness as a quick fabrication tool. For this work it would typically take several hours to pump down the equipment for use. The process is also inherently less controllable, as the deposition rate will depend on the amount of material present for the evaporation (as opposed to sputtering, where a known flux will be sputtered for a given power input). The high current needed to evaporate the material (typically in excess of 20 A) would vary and the deposition rate was not as easily predictable as the simple linear relationship between sputtered deposition thickness and time. However, it was possible to estimate the evaporated material thickness to an accuracy of around 50 nm, measured after deposition by stylus profilometer.

3.3.4 E-Beam evaporation

Electron-beam (E-beam) evaporation is similar to thermal evaporation but rather than directly using the thermal energy of a filament under high current to evaporate the target material, instead e-beam evaporation uses a charged tungsten filament to generate a beam of electrons. This beam is directed towards a target anode, evaporating part of that anode surface to a gas phase. The anode material then condenses onto the desired substrate surface (and all other surfaces inside the chamber).

Compared to the relatively rudimentary setup available for thermal evaporation as part of this research, the e-beam evaporation equipment gave substantially greater control over the deposition thickness and deposition rates onto the 3C-SiC epilayers. The Scientific Vacuum Systems Electron Beam Evaporation system was also fully automated, and a large variety of source materials were available meaning that multilayers of precise thickness (to an error of several angstroms) could be deposited if required. However, due to the process typically being much higher energy than thermal evaporation and the lack of a suitable heat sink within the e-beam setup significant issues were encountered with bake-on of resist. Figure 36 shows samples which used e-beam evaporation to deposit metal and experienced this bake-on issue. As such e-beam evaporation was not widely used throughout the course of this project. It was also deemed unsuitable for depositing MOS-stack capacitance dots as the wide selection of target materials introduced significant risk of cross contaminants being introduced into the oxide layers.

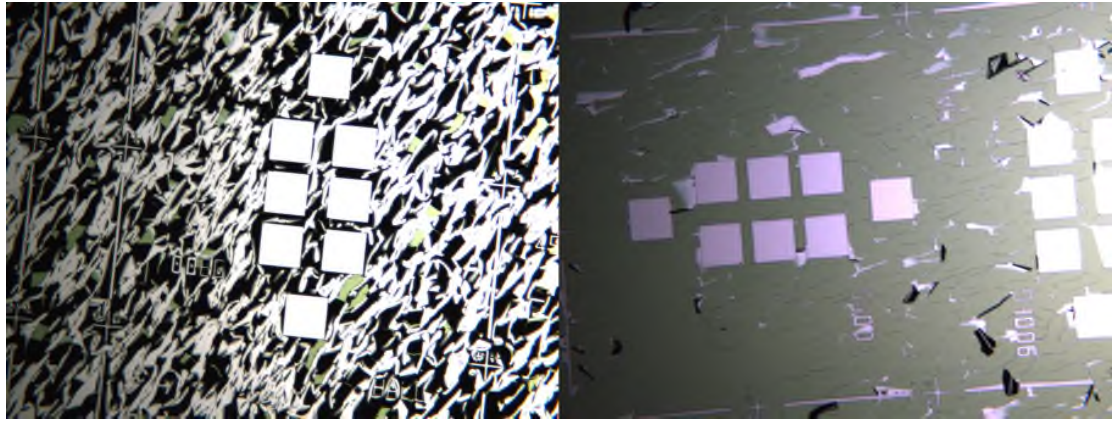


Figure 36: Sample with severe resist bake-on (L) meaning undesired metal was impossible to remove using conventional acetone lift-off. A light Ar^+ mill was used to attempt to remove this baked-on resist but did not completely remove it and left these devices unusable (R).

3.3.5 Thermal annealing

Thermal annealing is used to make contacts that are otherwise non-ohmic exhibit ohmic behaviour over a large enough current range to be practically useful. Generally speaking, the methodology for thermal annealing is very similar in many studies. Samples are heated in a dry, non-oxidising atmosphere, to a temperature which allows sufficient diffusion at the metal/semiconductor interface that an alloy is formed, and in the ideal case the Schottky barrier is reduced to zero. Fermi-level pinning restricts the possibility of this, however (as discussed above), meaning that even a metal or alloy with a very similar work function to the semiconductor cannot be annealed to provide a completely ohmic contact. However, thermal annealing is a routine part of semiconductor device manufacturing and in this work this technique was used to attempt to create device contacts that were sufficiently ohmic to allow the various properties of the 3C-SiC to be examined. Annealed and non-annealed devices cleaved from the same samples were compared.

Developing a methodology for annealing contacts was important in this research to facilitate measuring the mobility and Hall coefficient of doped 3C-SiC. A current range of around $\pm 0.3 \mu\text{A}$, and a voltage of $\pm 5 \text{ V}$ was applied during Closed-Cycle Cryostat (CCC) measurements (see section 5.3.1). During these measurements the temperature of the sample was reduced to around 30 K, so it was important to ensure that the contacts remained ohmic at reduced temperatures as well – typically as the temperature of the sample dropped, the resistivity would increase and contacts would become non-ohmic. As the temperature decreases, carrier concentration in the epilayer also decreases, leading to a higher resistance. Carrier concentration decreases with decreasing temperature as a

reduced thermal energy means that carriers can no longer be excited out of donor or acceptor sites (they are “frozen out”); there are therefore fewer carriers present in the material and hence less are available to conduct across the metal/semiconductor interface. Decreasing temperature also means that the energy barrier between the metal and the semiconductor, which previously carriers could cross as they had sufficient thermal energy, now require tunnelling to cross; the probability of this occurring is significantly lower. Annealing of contacts acts to reduce the energy barrier as an alloy is formed at the interface, meaning that in the ideal contact carriers can cross easily from one material to the other even at significantly reduced temperatures.

Figure 37 compares the I-V curves of the same unannealed sample (17-637, see section 5.3) at both 300K (representative of an upper bound for room temperature) and at reduced temperatures, as measured on a temperature-controlled probe station. At 300K the IV curve is completely linear over the applied current range ($\pm 0.3 \mu\text{A}$), but the current range over which the contacts are ohmic decreases rapidly with decreasing temperature. The contact resistance also increases dramatically such that the devices are no longer suitable.

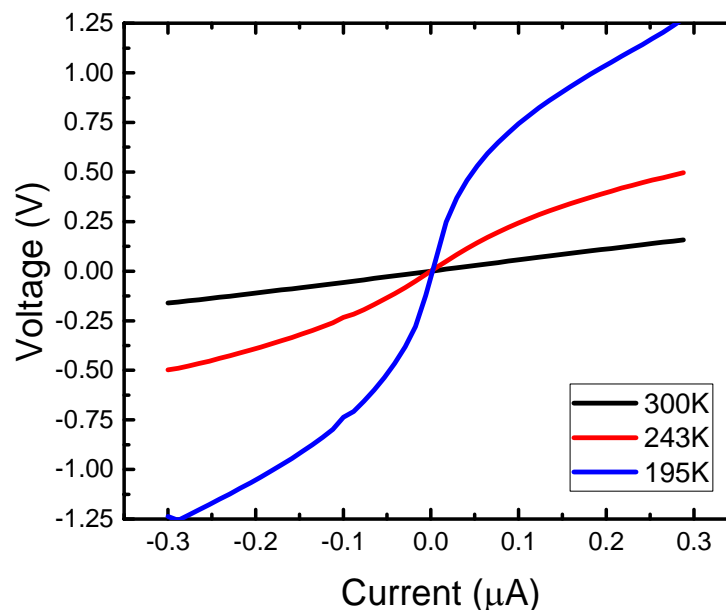


Figure 37: Room temperature (300 K) and reduced temperature IV sweeps of unannealed Hall bar contacts.

Initial tests to determine whether thermal annealing of the NiCr contacts would improve their low-temperature ohmic behaviour were unfortunately of limited success. This was mainly due to the rapid oxidation of the contact metals, which prevented adhesion of Al or Au wires when attempting to mount and wire the devices into chip packages. Due to the design of the CCC, chip packaging devices in this matter is necessary and hence as

the contacts could not be wired to the package, these devices could not undergo CCC analysis.

All thermal annealing was performed in a quartz tube furnace under a constant flow of Ar. Data from Colston's work suggested that the optimum temperature for annealing NiCr was 800 °C, so this temperature was chosen for these initial tests²⁵. The samples were inserted into the end of the tube furnace cold, and N₂ was passed through the tube at a constant rate of 5 slm while it was ramped to 600 °C. Here the samples were pushed into the centre of the tube where the temperature reading is most accurate. From this point the flow was switched to Ar and the furnace ramped up to the anneal temperature. Ar was used to minimise the chance of any unintentional N-doping of the 3C-SiC. N is a shallow donor so the introduction of unintentional dopants will significantly impact the electrical behaviour of the samples^{73,74}. Once this temperature was achieved, it was held constant for 450 s and the devices then removed. The NiCr was seen to oxidise extremely rapidly when the oxidation tube was opened to the air (to move the samples within the tube), despite the 5 slm Ar flow which should have minimised any back flow of air into the tube. Figure 38 shows samples with post-anneal oxide present. This oxide was not characterised but is likely to be a combination of various Ni and Cr oxides such as NiO and Cr₂O₃.

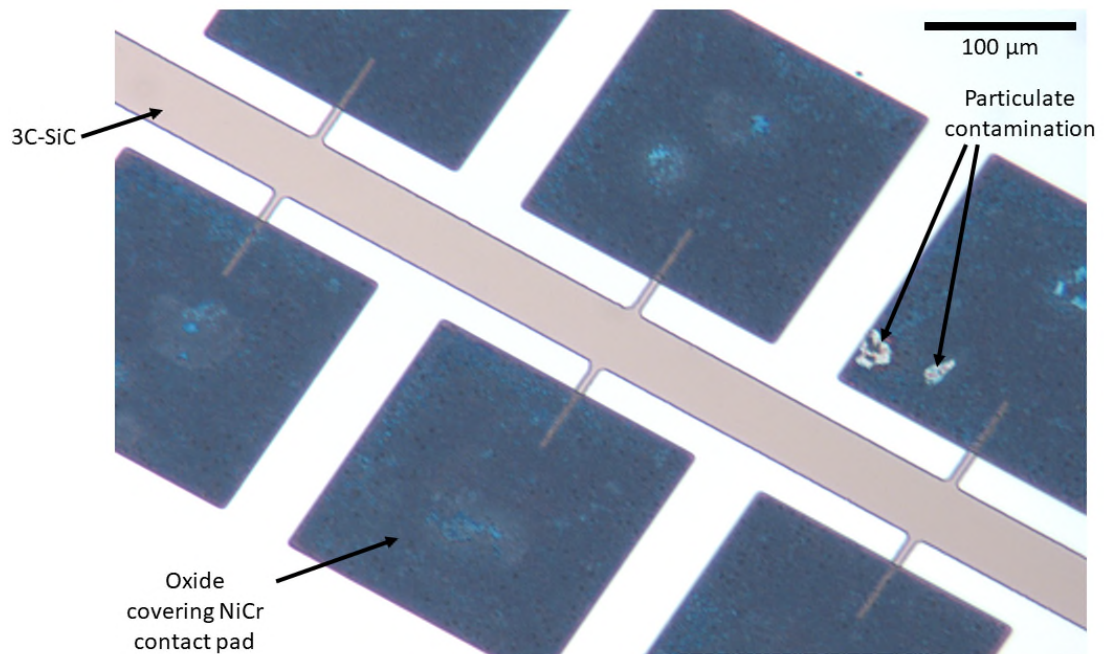


Figure 38: Hall bar samples showing oxide layer entirely covering NiCr contacts.

An attempt was made to further minimise the possible introduction of oxygen from the air by inserting the devices into the centre of the tube cold and ramping the temperature

both up and down while keeping the tube closed. While this ensured that no air could back flow into the tube when the end cap was removed to move the devices, the error on the measurement of the anneal time was greatly increased. Thermal annealing of NiCr to 3C-SiC can begin to occur at temperatures as low as 300 °C⁷⁵ so the error inherent in measuring the anneal time at a stable temperature was already large, but by starting the devices at the cooler end of the tube and moving them into the centre at an elevated temperature some control over this error was exercised. In keeping the tube closed throughout this was not possible. The samples annealed in this manner still oxidised extremely readily, suggesting that the gas sources (either the N₂ or Ar) contained a sufficiently large amount of oxygen to facilitate this oxidation. It is unlikely that the oxide could have formed from oxygen implanted during the metal deposition stage which was brought up to the surface by diffusion when heated, as the oxide layer formed was thick and visible on the surface. Metal deposition could not have introduced enough oxygen to cause this.

An easy resolution to the issues encountered in this work would be to anneal in an atmosphere of sufficiently pure N₂ or Ar, in a closed furnace. Forming gas (a mixture of Ar and hydrogen) may also be suitable. Alternatively, if a sufficiently high vacuum could be produced inside the furnace this would be suitable. As the other steps in the device fabrication process were successful and potentially suitable devices were fabricated, this is the final hurdle to assessing the electrical properties of this heteroepitaxially grown 3C-SiC. Given more time this would have been achieved within this research and should be an easy first step for a future project.

3.4 Reactive-Ion Etching (RIE)

Etching the mesa structures is a vital step in the fabrication of Hall bars and Van der Pauw crosses. The sole method for this within the scope of this project was by RIE. 3C-SiC is highly resistant or is indeed completely inert to most wet etchants but RIE has been shown to be highly effective. Many former projects within the Nano-Silicon group and the Engineering department within the University of Warwick have used RIE to define such structures⁷⁶ and so the processes are well established and have been automated. A Corial 200IL Inductively Coupled Plasma (ICP)-RIE reactor was used for all mesa definition. This was located within the University's Engineering cleanroom.

Sulphur hexafluoride (SF_6) was used as the etchant for all RIE. The physical process is similar to sputtering, where the surface of the sample is bombarded by high-energy ions, but in RIE the ions are highly reactive with the sample material. This results in layers being progressively etched away until the desired depth is achieved. Commercially available photoresists can be used to protect desired areas of the sample surface. Mesa structures were formed by protecting the intended mesa and allowing the rest of the sample surface to etch away. Metal contacts are also highly resistant to the SF_6 . RIE is a highly anisotropic process, so the side walls of the etched mesa structures are typically very straight and regular.

3.5 Cleanroom conditions

For any semiconductor device fabrication it is essential to control particulate and chemical contamination. Contamination was of particular concern within this research as this may result in device-killing issues, for example introducing particulates that may introduce additional charge trap sites into the dielectric oxide layer. Such contamination could cause the leakage current to be so high as to render the device unusable. At the fabrication scale in this work chemical contamination is only really a concern during epitaxy, annealing, and oxidation of material. Physical contaminants (i.e. particulates) can cause severe issues with the photolithographic processes, adhesion of metal contacts, etc. which again are potentially disastrous.

As such, rigorous processes and controls were put in place for this work to minimise any potential contamination. Principal among these controls was the ISO Category-5 cleanroom in which the majority of all device fabrication processes took place. As defined by ISO 14644-1, a Category-5 cleanroom is one in which the maximum number of particles of diameter $\geq 0.1 \mu\text{m}$ in a square metre of air does not exceed 10^5 ⁷⁷. Particulates in this environment are chiefly controlled by a controlled airflow involving HEPA filters, an air shower on entry, and use of cleanroom clothing (gowns, caps, boots etc) by all cleanroom users. In addition to these processes and controls, wherever possible all devices were stored in vacuum containers which had been backfilled with inert gas (typically Ar) before being pumped down. This limited the devices exposure to oxygen, which was particularly important for the MOS devices. Standard handling practices were

also observed, i.e. all wafers were stored in clean and sealed wafer trays, all devices were handled solely with clean tweezers, etc.

4 Material analysis

4.1.1 X-Ray Reflectivity (XRR)

X-Ray Reflectivity (XRR) is an X-ray characterisation technique often used to analyse the thickness, density, and surface roughness of thin films. The intention of using XRR in this research was to quantify the thickness of grown oxide layers and from that data extrapolate a growth rate for the oxide. A Panalytical X'Pert Pro MRD high resolution X-ray diffractometer was used for all XRR measurements in this work.

XRR relies on reflecting X-rays off a sample at a “grazing angle” θ , which is below the critical angle of the material θ_C . If $\theta < \theta_C$, all incident X-rays will be reflected with a take-off angle equal to that of the incident angle, for a perfectly flat surface. Figure 39 shows a diagram of this setup.

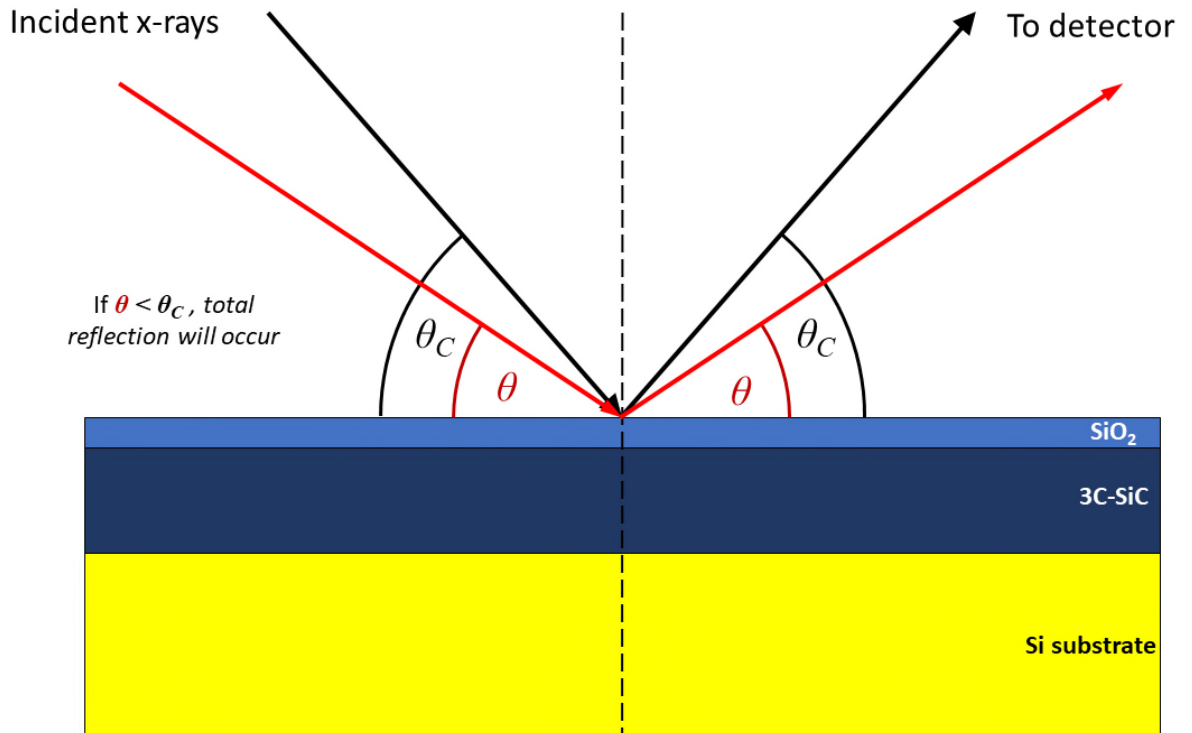


Figure 39: Diagram showing specular reflection during XRR experiments. Critical angle is denoted by θ_C . For a given sample, the critical angle is identified by taking several low-resolution scans and identifying the areas of peak intensity; the most appropriate range for θ can then be

determined. The diffractometer rotates through θ across this range and the intensity of the reflected X-rays is measured. As no sample surface is perfectly flat, some scattering occurs – therefore the intensity curve generated from the detected X-rays will have a characteristic profile. From the different features of this profile, parameters for the sample can be determined. For example, a periodic oscillation in the intensity curve relates to the thickness of the sample; thicker samples will show a much smaller oscillation period than thinner ones. The location of the critical angle θ_C will also affect the shape of the intensity curve, changing the position of the first shoulder that is observed with increasing scan angle θ . As the critical angle is dependent on the refractive index of the material, which in turn is dependent on its density, the density can be calculated. Similarly, surface roughness and interface roughness (for multiple-layer materials, such as the samples featured in this work) can be calculated by examining the decay rate of the reflected X-rays and the amplitude of the oscillation respectively⁷⁸. While all of these parameters can be determined independently, in practice they are all calculated concurrently using a fitting algorithm – in this work, X'Pert Reflectivity software was used. This software is produced by the manufacturers of the diffractometer.

The Reflectivity software uses a fitting algorithm to attempt to generate a curve which fits the measured intensity curve; from this simulated curve it can then calculate the different material parameters. This algorithm uses a combination of parameters input by the operator and known values drawn from an internal materials library. The operator can define the known structure of the sample using this materials library; for example in this work the 3C-SiC epilayer was known to be (001)-oriented and the thickness was known to a high degree of accuracy so this was input, along with the orientation and thickness of the Si substrate.

Aiding the fitting algorithm is the ability to limit the parameters to a particular range. Interface roughness was factored into this algorithm based on estimates from AFM performed on similar samples, grown by CVD using the same technique⁷⁹. Density estimates were obtained from literature sources²⁸. AFM was later performed on the non-oxidised material and showed good agreement with these estimates (see section 4.1.3). Surface roughness was not limited in the fitting but again showed good agreement with AFM data. The ranges applied to the algorithm were iteratively reduced in order to optimise the fit and the oxide thickness measurements extracted by the software. Figure 40 shows the real and simulated curves for two samples.

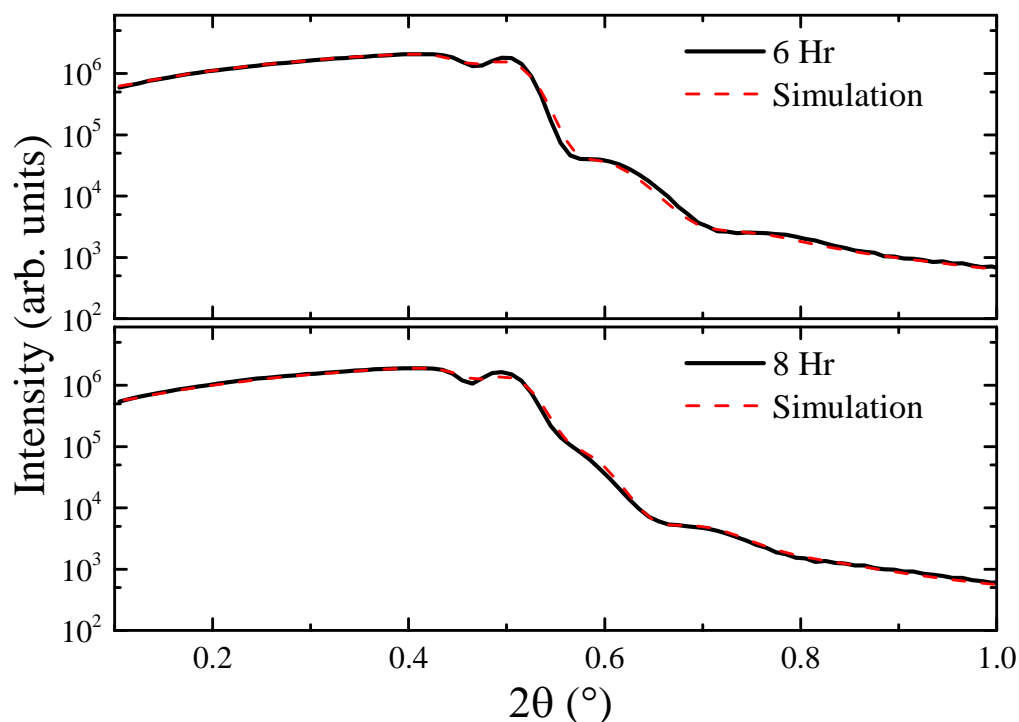


Figure 40: Example of real curves generated from 2θ scan as compared to simulated curves. Thickness measurements were extracted from these simulations.

A limitation of this method is that the software does not produce any meaningful measure of how close a fit the simulated curve is. It is therefore reliant on the operator to determine when a fit is sufficient which introduces error. In this work the total error in the oxide thickness as calculated from XRR data is suggested to be around 10%. This is likely to be an over-estimate. This figure was determined by comparing XRR to another technique used for measuring film thicknesses; Fourier-transform infrared spectroscopy (FTIR). FTIR can detect film thickness variation as little as several nm, but typically requires a film of at least 300 nm in thickness in order to be reliable. FTIR is routinely used to inspect the small variations present across an epilayer grown by CVD for very similar materials²⁵. XRR is also used in this material characterisation as a complementary technique, and comparison of the two data sets a maximum error of around 10%⁸⁰. In this way FTIR can be considered as calibration for the XRR technique. However, as it has not been possible to quantify the absolute error, the thicknesses calculated from XRR measurements (and therefore the oxidation rate extracted from them) can only be considered indicative. As such other techniques (see sections 4.1.2 and 5.2.1) were used alongside XRR to determine the oxide thickness.

The XRR data across all samples (shown in Figure 41) suggested that the oxide growth rate is effectively linear after a short initial period (0 – 10 nm). The fitting model used by the Reflectivity software could not accurately model the oxide thickness below approximately 10 nm, and these points have not been included in the linear fit calculation and are marked in red. However, according to the Song model (see section 2.1), initial oxidation should be rapid and stabilise to a linear growth rate within the first several nm of growth ⁵¹. This linearity is suggested in Figure 41 as the linear fit is negative at a thickness of 0 nm; the oxidation rate must therefore be greater in the initial period (0-2 hours). The oxidation process is dependent on the rate of O₂ diffusion through the oxide as it forms as per Fick's law ³³, and so is highly dependent on temperature; as such it is expected that reducing the oxidation temperature below 985 °C would drastically increase the oxidation time. Oxidation was relatively slow at 4.08×10^{-2} nm/min, around 2 orders of magnitude slower than SiO₂ grown on Si under the same conditions ⁴⁸, which is likely due to the higher bond energies of Si-C bonds present in SiC compared to Si-Si bonds in Si ²⁸.

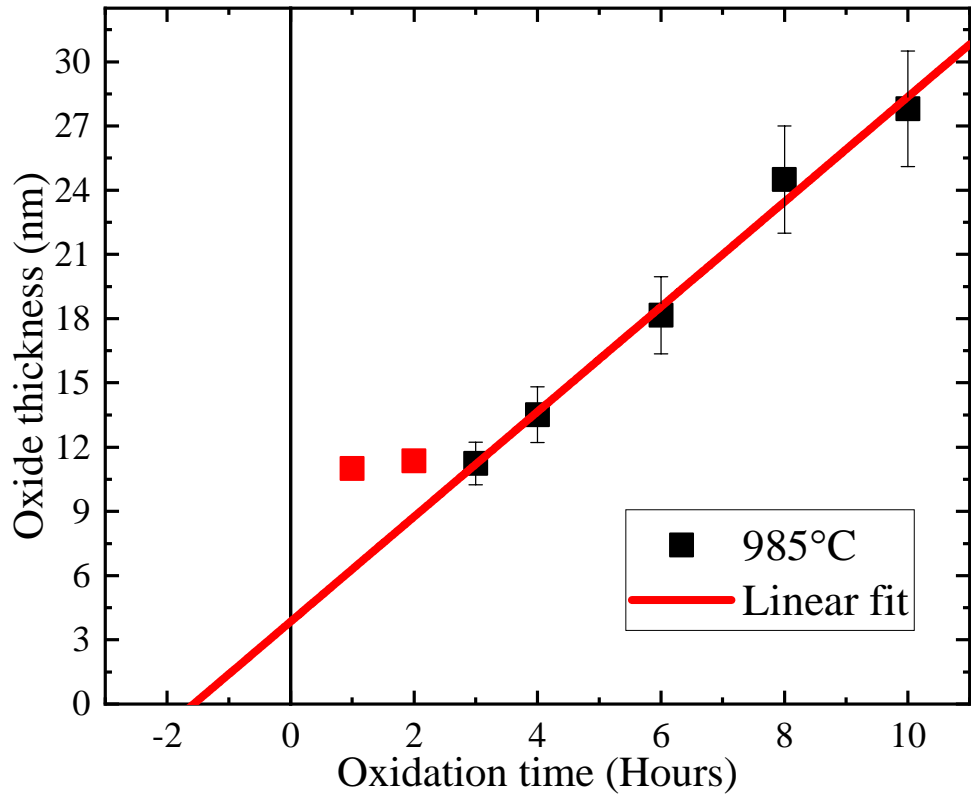


Figure 41: SiO₂ growth rate on 3C-SiC epilayer at 985 °C in O₂ ambient. The linear fit showed the oxidation rate to be 4.08×10^{-2} nm/min, approximately 2.5nm/hr. The error on all points from 3 hr oxidation onwards was assumed to be 10%, prior to this the error was much larger due to limitations of the model.

It has also been shown that SiO₂ growth on 4H-SiC is highly dependent on the formation layer orientation: at 950 °C the rates can differ as much as 1.2×10^{-2} to 18.2×10^{-2} nm/min on the Si- and C-terminated faces respectively⁴⁷. Like 4H-SiC, 3C-SiC may have either Si- or C-terminated faces dependent on crystal orientation. It is therefore expected that different orientations of 3C-SiC will oxidise at different rates, however, only (001)-oriented material has been investigated in this work. (001)-oriented 3C-SiC is always Si-terminated.

4.1.2 Cross-Sectional Transmission Electron Microscopy (X-TEM)

X-TEM is a powerful technique that allows for the molecular structure of a wide variety of materials to be directly observed and assessed, as it can provide magnification of up to 1,500,000 times. In this research X-TEM was principally used for qualitative assessment of grown oxides and verification of their thickness. This data was used in conjunction with C-V and XRR analysis to determine oxidation rates.

The specifics of how TEM works are beyond the scope of this thesis, and the reader is directed to Williams and Carter's *Transmission Electron Microscopy: A Textbook For Materials Science* for a comprehensive explanation of these physical mechanisms⁸¹. By way of a brief explanation, an electron gun and a series of condenser lenses are used to direct a beam of electrons onto a sample. Some electrons will pass through the sample (the "direct beam") and, if the sample is crystalline, some will be diffracted. The diffracted and direct beams are then focussed and projected onto a fluorescent plate. The resultant photons are detected by a charge coupled device (CCD) to generate a digital image. The diffraction pattern of the crystal and, by the introduction of an objective lens, an image of the sample can be observed. An objective aperture is also used to selectively observe either the direct or diffracted beams. These make up the two main image types: bright-field (BF) and dark-field (DF) images. If the direct beam is used, the image is BF. If the diffracted beams are used, the image is DF. The objective aperture can be used to select a particular crystallographic plane; as such DF images are typically used to inspect the crystal structure of a sample, including strain effects and defects that may be present. A drawback to using DF images is that it relies on diffraction in the sample, so any amorphous or polycrystalline material will be dark in the image. Conversely a BF image will typically show all features of a sample regardless of crystallinity but will not provide

as much crystallographic information. A third imaging type is sometimes used for high-resolution TEM (HR-TEM) which is similar to BF but rather than only selecting the direct beam the objective aperture is much larger and allows the direct beam and several diffracted beams through. The image is formed by the interference of these beams; this is known as phase contrast.

As X-TEM requires a material which is nearly atomically thin, several processes must be employed to correctly prepare samples for imaging. First is to cleave samples to a suitable size; this makes the grinding and polishing stages easier and minimises wastage of material. All samples prepared in this manner were approximately 10x15 mm. It is necessary to affix two such samples together, and then back both with a piece of waste Si wafer of the same size. Standard two-part epoxy is used to bond all these together. The stack is then clamped in a vice and heated on a hot plate to cure the epoxy, and once cured the stack is cut in two lengthwise. One half is taken to be further processed and the other retained in case preparation fails on the other sample or further samples need to be prepared from the same material. These initial processes are all laid out in Figure 42.

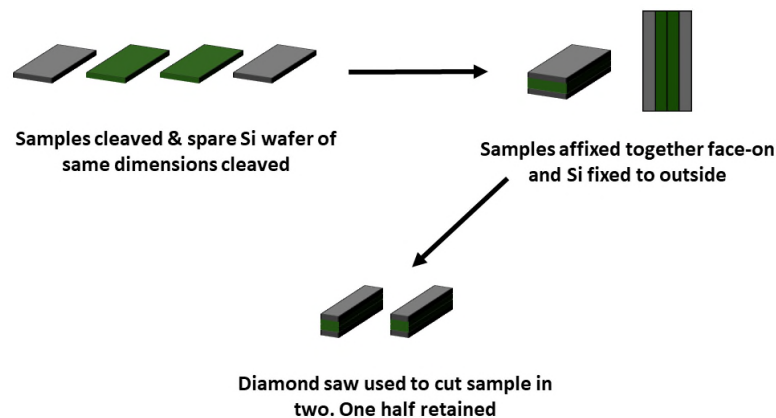


Figure 42: Initial sample cleaving & preparation.

The next step is to create a very flat, smooth surface to one side of the sample. The sample is affixed to a metal block using temporary mounting wax and mechanically polished until smooth. 3C-SiC is an extremely hard material (~9.8 Mohs hardness²⁶) so amorphous SiC grinding paper was used with a variety of different grits. The smooth surface that results allows for the sample to be polished very thin.

The sample is then mounted onto a glass slide, smooth side down, and again ground and polished using a series of increasingly high-grit SiC grinding papers. The intention here is to polish the sample to a very low thickness; on the order of tens of microns. Once

sufficiently thin, copper rings are affixed to the sample using two-part epoxy, the remaining material scratched away, and acetone is used to dissolve the mounting wax. This leaves a very thin cross-section of the material contained within a copper ring which will fit in the sample holders used by the transmission electron microscope. Figure 43 shows these steps.

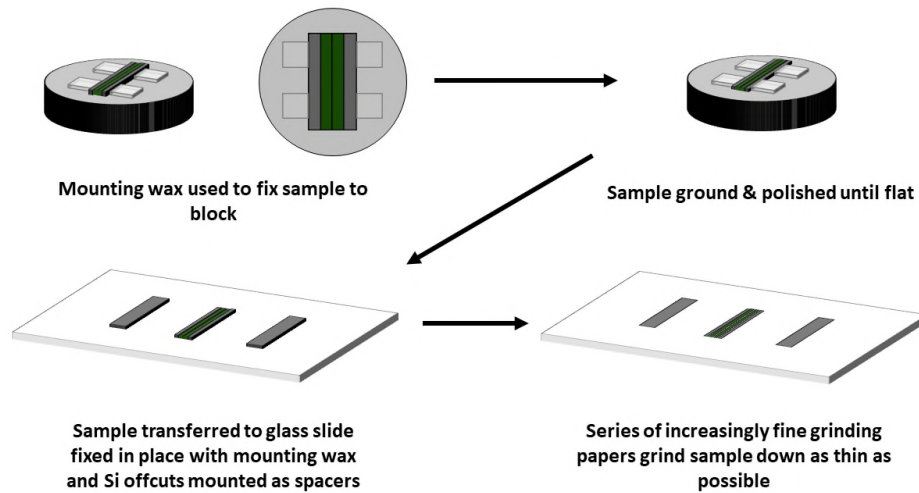


Figure 43: Mechanical polishing process.

Although very thin, the sample needs one final process in order to make it atomically thin and hence suitable for X-TEM. A precision ion polishing system (PIPS) uses two highly energetic ion beams to sputter away material at the interface between the two sample edges. These beams are angled such that eventually a small hole is formed at this interface. The very edge of this hole is at most only a few atoms thick, which is thin enough that X-TEM can be performed on the sample. It was found that it was also advantageous to subject the samples to a lower-intensity, defocussed ion beam at the end of the PIPS process in order to polish away some of the damage that PIPS does to the sample and clean up the edges, making for better images.

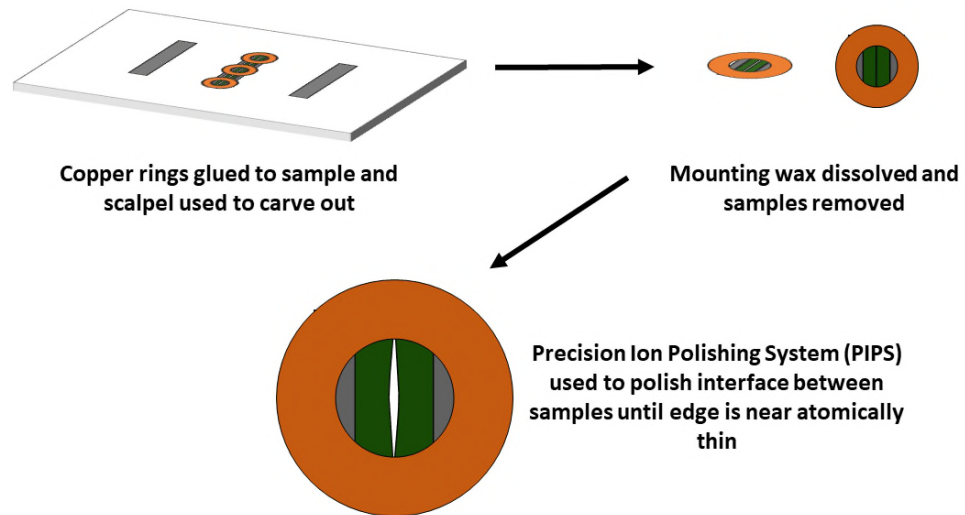


Figure 44: PIPS process, leaving sample prepared for X-TEM measurements.

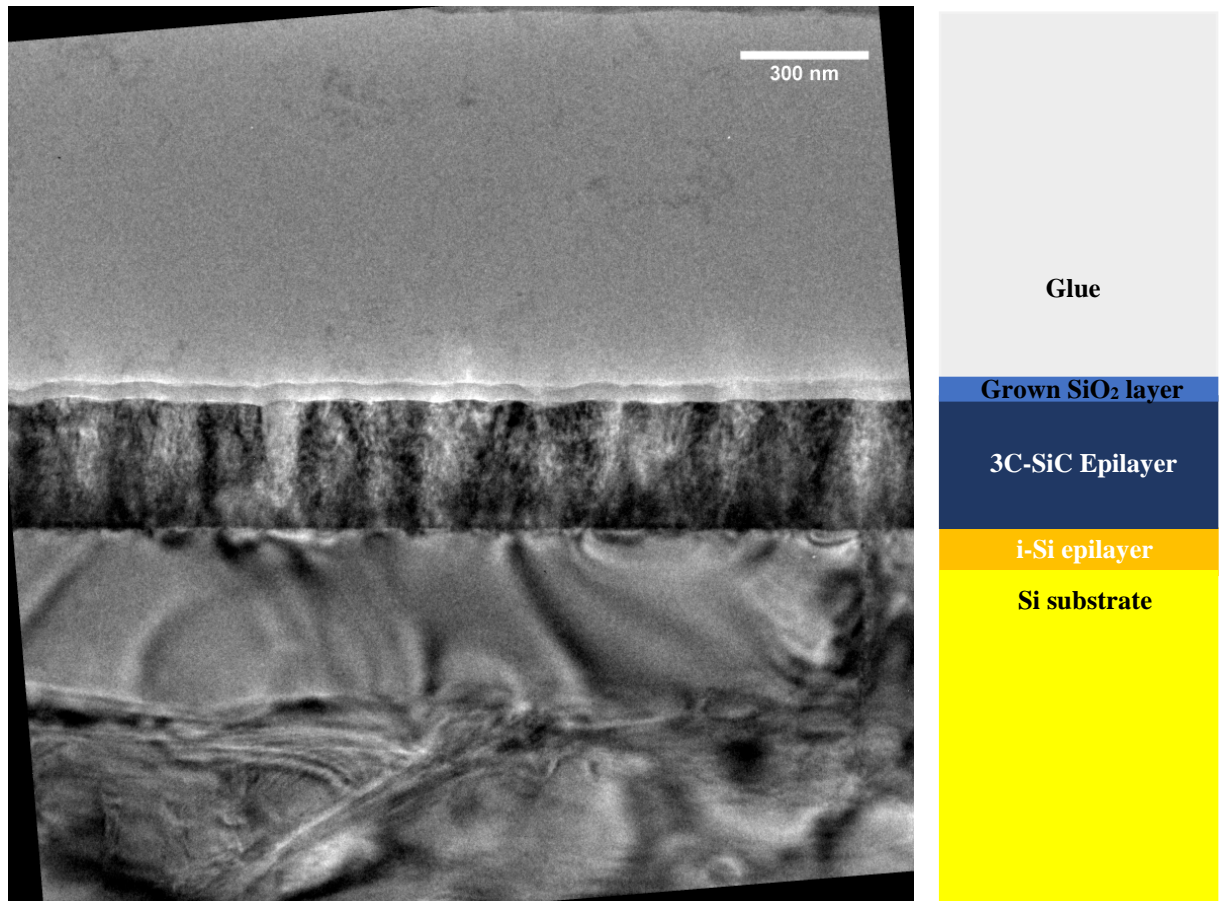


Figure 45: (L) Cross-sectional BF image of 3C-SiC epilayer on Si substrate and (R) cross-sectional diagram of layers. This sample was oxidised for 10 hours at 995 °C.

Figure 45 shows an example of the BF X-TEM images taken as part of this research. The oxide layer, fully relaxed 3C-SiC epilayer, and the intrinsic silicon (i-Si) layer can be seen. This image was obtained from a sample which had undergone oxidation for 10 hours

at a slightly higher temperature than that performed for most of this work (995 °C as opposed to 985 °C) and as expected the oxide observed is much thicker than that grown by lower-temperature oxidation. XRR data for the sample agrees well with the thickness estimates obtained from the X-TEM images. This technique is limited by the fact that only a very small area of the sample is imaged. Care was taken to ensure that the images taken were truly representative by examining the entire sample and only measuring the oxide thickness if it was observed to be very uniform across the entire 3C-SiC layer. In practice all the samples showed high levels of uniformity. This technique does however rely upon the experience of the microscope operator to identify and discard phenomena such as damage incurred during the PIPS process. This may explain some of the scatter seen in Figure 47. Future work could improve upon this by taking more images at different points across the sample and averaging the measured oxide thicknesses.

The SiO₂ layer is shown in these images to be homogenous and of even thickness, following the morphology of the 3C-SiC epilayer surface. The SiO₂ layer does not appear to have a high defect density and the defects seen in the 3C-SiC epilayer do not appear to propagate into the oxide layer. The difference in structure of the crystalline 3C-SiC and the amorphous SiO₂ is evident in Figure 45. It also appears that the interface between the SiO₂ and the 3C-SiC epilayer is sharp; i.e. there is little to no graduated area between the grown oxide and the 3C-SiC. This is expected in accordance with the Song-corrected Deal-Grove model ⁵¹.

Qualitative assessment of the oxide layers was much the same for all samples; all images showed an amorphous oxide which was of even thickness, followed the surface morphology of the 3C-SiC epilayer, and did not have any apparent defects that propagated from the epilayer. Using X-TEM to measure the oxide thickness gave results very similar to that obtained by XRR measurements, with the advantage that the thickness was measured directly rather than estimated by fitting a simulation to the recorded data. This overcame the issues with simulating very thin (>10 nm) oxides. The only sources of error in this technique were the human error in determining distances between the SiO₂/3C-SiC and SiO₂/epoxy interfaces and the human error in calibrating the distance measurement in the imaging software. All calibration was performed using the Si lattice spacing from the Si observed close to the Si/3C-SiC interface. Figure 46 shows an example of this calibration.

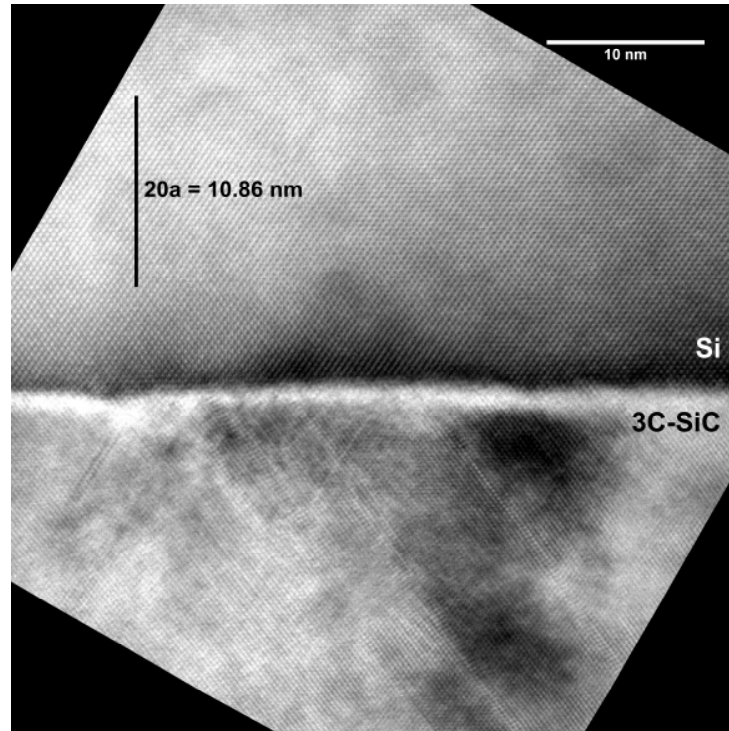


Figure 46: High-resolution image of Si/3C-SiC interface used for calibration. 20 Si lattice spacings are measured and this known value is used to calibrate all images.

BF images were used to determine the oxide thickness as they had significantly better contrast than ST images. Figure 47 shows BF images of samples oxidised for between 1 and 8 hours with the thickness of the oxide layers marked. Such oxidation times are much longer than would be typical for Si at equivalent temperatures (see section 4.1.1) but are similar to the standard oxidation times for SiC at around 1000 °C⁴⁸. The oxidation process is strongly temperature dependent and the oxidation rate directly proportional to the temperature, hence for the higher temperatures more typical for SiC oxidation, oxidation rate is much quicker. As the purpose of this research was to determine whether a high-quality oxide could be grown at low temperature (<1000 °C), no temperatures above 1000 °C were explored.

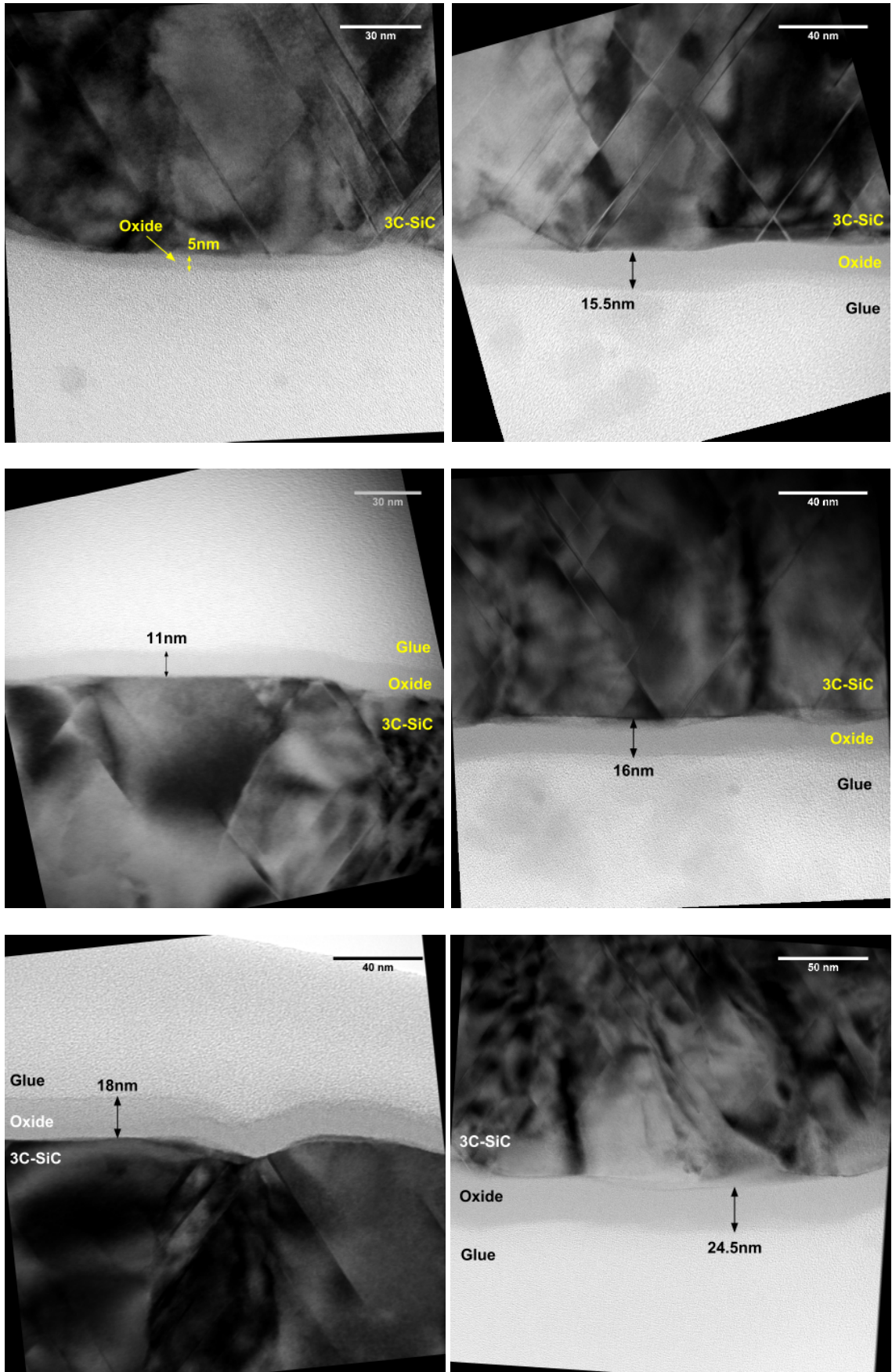


Figure 47: BF images showing oxide thickness measured for samples of varying oxidation time. Top: (L) 1 hour (R) 2 hours. Middle: (L) 3 hours (R) 4 hours. Bottom: (L) 6 hours (R) 8 hours.

Oxide thickness as a function of oxidation time is plotted on Figure 48, along with the same measurements from XRR models. The two methods show largely similar results, and interestingly shows that the 2hr sample had a significantly thicker oxide than the trend suggests. It is possible that this sample was in a slightly different position within the furnace and hence was subject to a higher temperature than the others. It also explains why this point was initially difficult to model using the XRR software as the actual thickness lay well outside of the expected parameters (and hence the limits placed on the model). For both sets of data the oxidation rate was calculated to be approximately 4×10^{-2} nm/min.

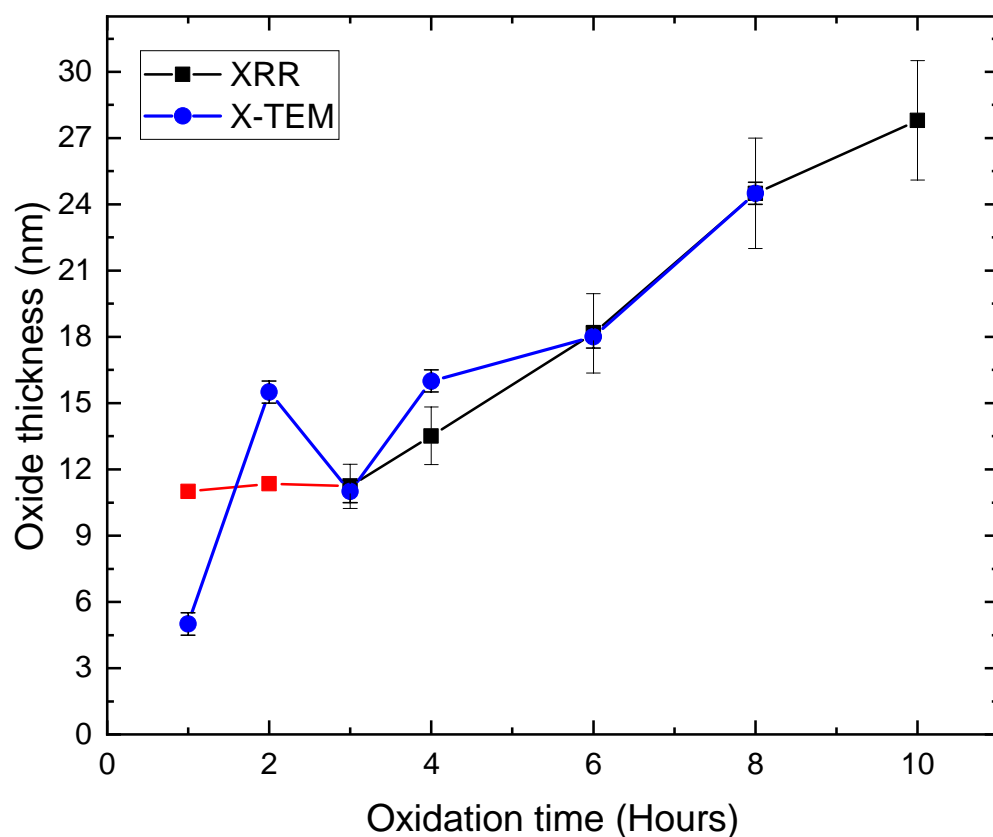


Figure 48: Oxidation rate for 3C-SiC using dry oxidation at 985 °C. XRR and X-TEM data is presented and shows congruence between the two methods. Error in X-TEM measurements is 0.5 nm.

Alongside their usefulness for determining oxide thickness, BF images were used alongside DF images to assess the crystallinity of the oxide layers. As discussed above DF images do not show non-crystalline material, so by comparing the BF and DF images it was possible to verify that the oxide grown was amorphous. This was also evident in the high-resolution images, although was less obvious. High-resolution images were used primarily to calibrate the image manipulation software and to qualitatively assess the oxide, as the lower contrast between the oxide and epoxy layers made it difficult to

accurately determine oxide thickness. Some images, such as Figure 49, did show a clear distinction between these layers. High-resolution images were also useful for directly observing defects in the 3C-SiC layer and whether these defects propagated into the oxide. Figure 49, of the 8 hr sample, shows several stacking faults and microtwins and clearly evidences that these faults terminate at the 3C-SiC/SiO₂ boundary. It is worth noting that the defect density at the Si/3C-SiC interface is much higher than that at the 3C-SiC/SiO₂ interface as the defects largely annihilate, meaning that those remaining in the 3C-SiC surface are not necessarily the “device-killers” that particularly stacking faults are often regarded as^{82,83}.

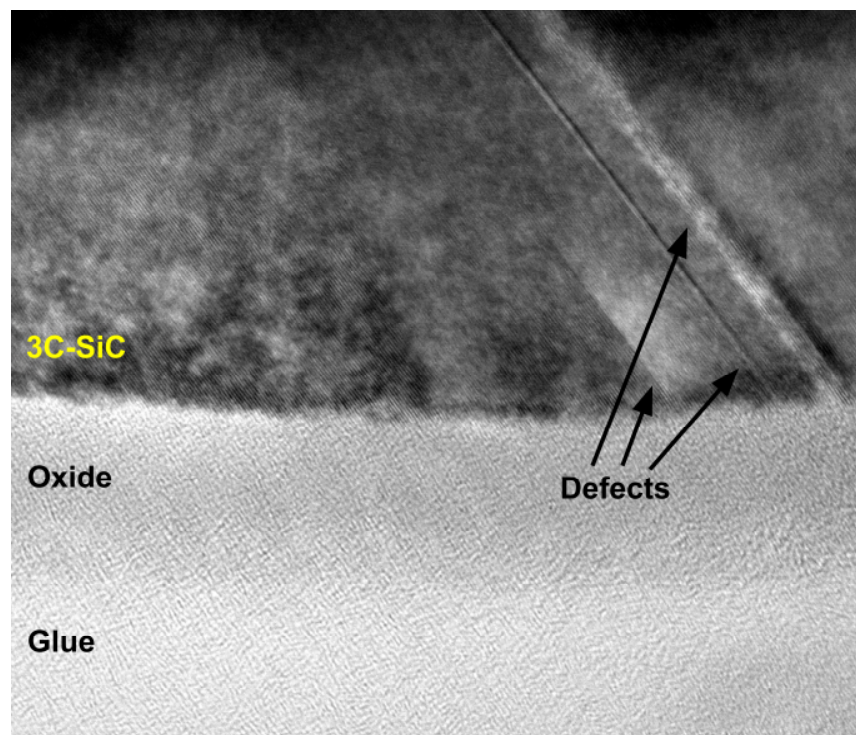


Figure 49: HR image of 8 hr sample, showing the oxide layer and surface-breaking defects in the 3C-SiC. The defects do not propagate into oxide.

4.1.3 Atomic Force Microscopy (AFM)

While the X-TEM images suggested that the grown oxide closely follows the surface morphology of the 3C-SiC epilayer, each image is only of a very tiny cross-sectional slice of the surface. This being the case it was necessary to perform atomic force microscopy (AFM) scans of the samples to quantify whether the oxide was contributing to the surface roughness of the samples. One of the most widely-used parameters used to describe surface roughness of any material is the root mean square (RMS) roughness often denoted

by R_q . This is effectively the standard deviation of the distribution of surface heights and does not distinguish between peaks and valleys on the sample surface. Within this research we are only interested in an absolute value for the surface roughness with which we can compare samples, so RMS roughness is an appropriate measure of this. It is a statistical measure which is by no means confined to AFM measurements, and can be expressed as

$$R_q = \sqrt{\frac{1}{L} \int_0^L Z(x)^2 dx} \quad (28)$$

where L is the length of the raster sweep and $Z(x)$ is the deviation from mean height of the surface, as measured by the AFM cantilever⁸⁴. As equation 25 shows, RMS roughness is (as the name suggests) the square root of the arithmetic mean of height values, and so this measure can be susceptible to error when a particularly large peak is erroneously encountered, for example by physical contaminants on the sample surface. In this work the data analysis program Gwyddion was used to calculate the RMS roughness values. For each sample the software calculated R_q across each row of pixels and calculated the average to provide an average RMS roughness value for the entire sample surface.

In this work AFM was solely used to measure the RMS roughness of the oxide and 3C-SiC surfaces, but in general the technique can provide accurate images of surface structures to a sub-nanometre resolution⁸⁵. This resolution being below the optical diffraction limit means that AFM as a technique is comparable to similar technologies such as scanning electron microscopy (SEM) and is often used as a complementary technique. The advantage of AFM over SEM is that AFM can directly measure the dimensions of surface features in 3 dimensions.

For this work all AFM measurements were made using tapping-mode, one of several different AFM methodologies. This involves vibrating the cantilever at or near its resonant frequency, and rastering it across the sample surface. As the cantilever moves across the sample surface, electrostatic forces will change the amplitude of the cantilever's vibration. As the cantilever comes closer to the surface, a combination of repulsive (from Coulomb interactions) and attractive (from van der Waals interactions) forces will cause a net force on the cantilever tip. This net force will cause a reduction in both the amplitude and frequency of the oscillation of the cantilever. This force is not actually measured during tapping mode; rather, a feedback loop is used to constantly

monitor the resonance of the cantilever and to the adjust the height (z) of the cantilever with respect to the surface to maintain a constant amplitude. It is this change in z which is recorded with respect to the x - and y -coordinates of the cantilever and hence maps the surface morphology of the sample ⁸⁵.

In this work a range of samples with varying oxidation times were images using an Asylum Research MFP-3D atomic-force microscope, alongside an as-grown 3C-SiC epilayer as a control sample. Figure 50 shows a $5 \times 5 \mu\text{m}$ scan of the control sample, which was found to have an average RMS roughness of $4.8 \pm 0.05 \text{ nm}$. This roughness is representative of the typical surface roughness of 3C-SiC epilayers grown by low-temperature epitaxy, which is typically in the range of 2-10 nm ²⁵. Figure 51, Figure 52, and Figure 54 show scans under the same conditions for this 3C-SiC epilayer after 4-, 6-, and 10-hour oxidations respectively. As with other samples all oxidation was undertaken at 985 °C in a quartz tube oxidation furnace under ISO 5 cleanroom conditions.

As is evident from Figure 55, an increase in oxide thickness does not result in any significant change in surface RMS roughness, as the small deviations in measured values fall well within the error margins for the measurements. It should also be noted that the RMS value of the 10-hour sample was calculated from a $4.59 \times 4.77 \mu\text{m}$ scan, as this image was cropped slightly to remove a physical surface contaminant which was otherwise skewing the RMS roughness value. Figure 54 shows the full $5 \times 5 \mu\text{m}$ scan, evidencing the physical contaminant. The difference in error is negligible.

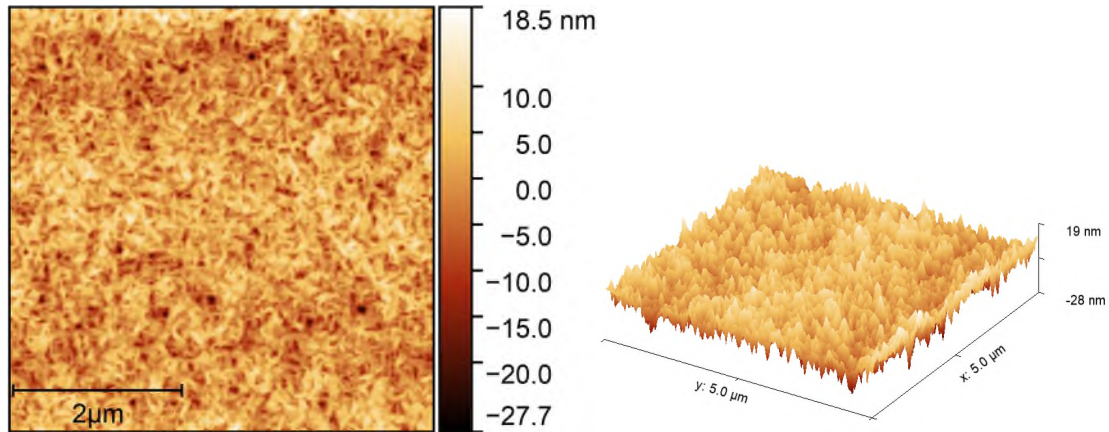


Figure 50: (L) Heatmap of surface roughness from AFM scan of as-grown 3C-SiC and (R) the same surface profile as a 3D plot.

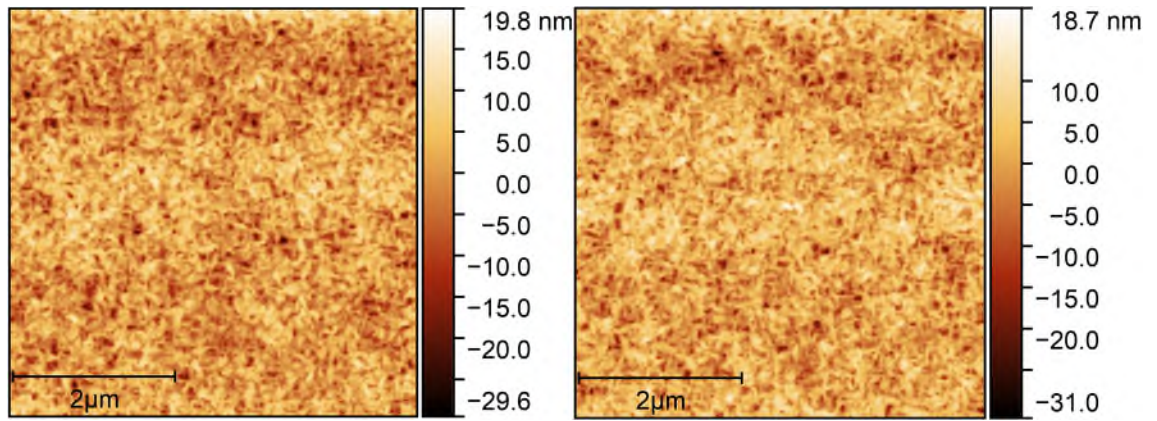


Figure 51: (L) Heatmap of surface roughness of 4 hour oxidised sample.

Figure 52: (R) Heatmap of surface roughness of 6 hour oxidised sample.

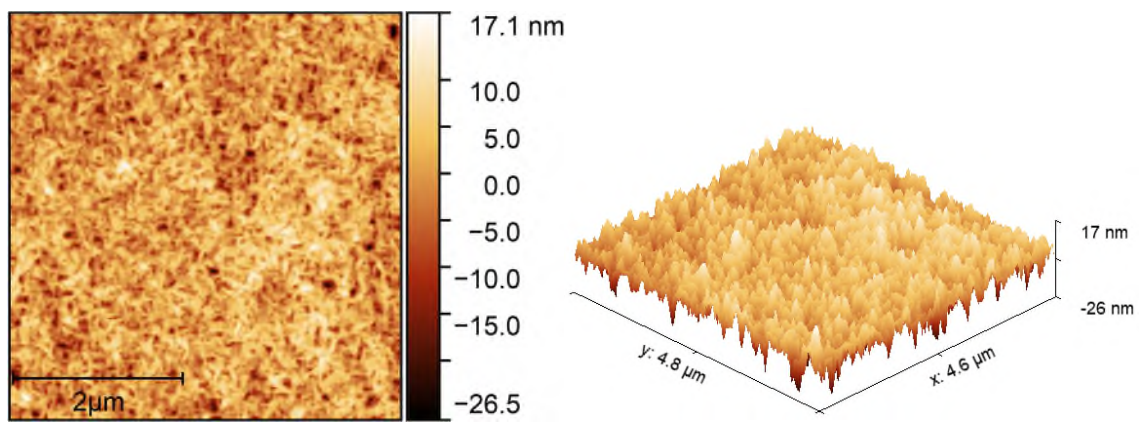


Figure 53: (L) Heatmap of surface roughness of the 10 hour oxidised sample and (R) the same profile as a 3D plot.

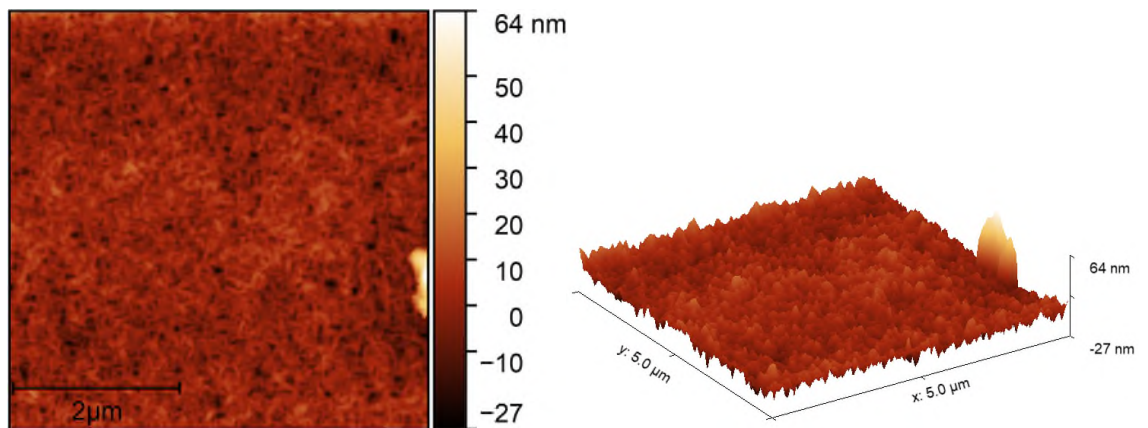


Figure 54: (L) Heatmap of surface roughness of the 10 hour oxidised sample and (R) the same profile as a 3D plot, with physical contaminant present on the surface. This data was not used to calculate RMS roughness.

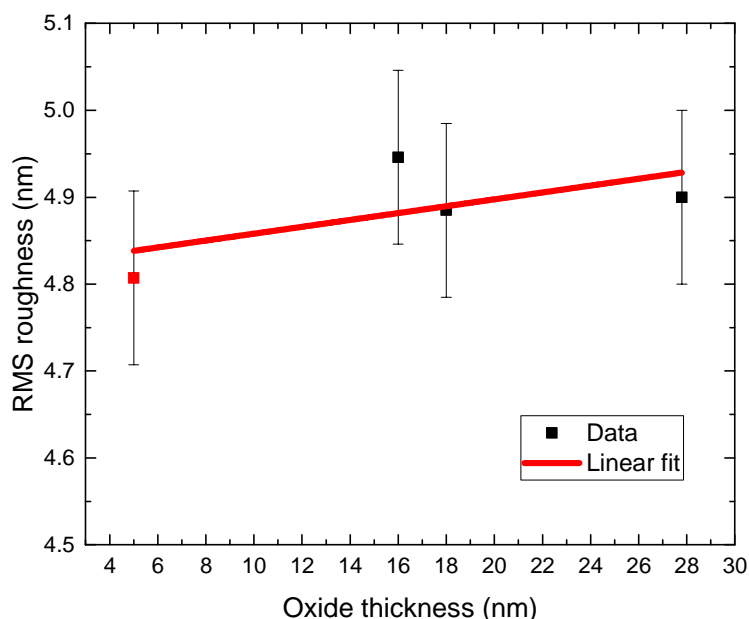


Figure 55: RMS roughness as a function of oxide thickness. Here oxide thickness has been determined by X-TEM as this was the most accurate measurement, excluding point 4 which was taken from XRR measurement (see section 4.1.1). As all deviation is within the error of each point, the slight positive gradient in the linear fit is not indicative of an actual increase in RMS roughness.

4.1.4 X-Ray Photoelectron Spectroscopy (XPS)

X-Ray Photoelectron Spectroscopy (XPS) is a powerful technique for quantifying the chemical composition of a material. A full explanation of the technique can be found in J. Watts and J. Wolstenhome's *An introduction to Surface Analysis by XPS and AES* ⁸⁶. Samples are bombarded with high-energy X-rays and the quantity and kinetic energy of the resultant photoelectrons are measured. The kinetic energy of the photoelectrons will relate exactly to the binding energy required to excite them from the sample surface, and so elements present in the sample can be identified. Not only can this provide detail of elements, but as chemical bonds will cause a change in the binding energy, various bonds can be detected and hence the proportion of compounds present in a sample. Typically this technique has a detection rate of parts per thousand ⁸⁶, and so while not as sensitive as, for example, SIMS (see section 4.1.5), XPS can be useful for identifying the major constituent parts of a sample (traces down to ~0.5%).

For this work, samples of various oxide thickness were analysed using a Kratos Axis Ultra delay-line detector (DLD) system. As well as taking data at the sample surface (i.e. the surface of the oxide layer), the Kratos' integrated Ar⁺ sputter gun was used to remove material from the oxide layer, until the oxide/3C-SiC interface was reached. In order to identify when the oxide had been milled to a sufficient depth, low resolution scans were

performed at regular intervals, increasingly frequently as the interface was expected to be reached (the approximate milling rate being known). The interface was identified by observing the reduction in the O peak and the corresponding increase in the Si and C peaks.

At this interface, scans of varying take-off angle (TOA) were performed. By varying the angle of the sample with respect to the incident X-rays, the material can be probed to different depths. The TOA, defined as the angle of the emitted photoelectrons detected by the detector relative to the normal of the sample surface, is ordinarily 90°. As the sample is rotated, the relative angle of incidence is varied, and so is the TOA. The further any given photoelectron must travel through the sample, the greater the chance that some sort of interaction occurs which prevents emission from the sample surface. The smaller the TOA, the greater the path length of any photoelectron laterally through the sample, and hence any photoelectron detected by the detector must have been emitted from a shallower depth (as those from greater depths are screened out by interactions within the sample). This is known as the information depth d_I . Defining the maximum path length (within the material) of an emitted photoelectron as d (i.e. the information depth at a TOA of 90°), the information depth at any other TOA θ can be defined as

$$d_I = d \sin(\theta), \quad (29)$$

as shown in Figure 56. d is roughly 3 times the electrons inelastic mean free path λ ⁸⁶ Photoelectrons will be emitted from the entire volume enclosed by the information depth and the cross-sectional area of the X-ray beam. The angle between the X-ray source and the photoelectron detector remains constant.

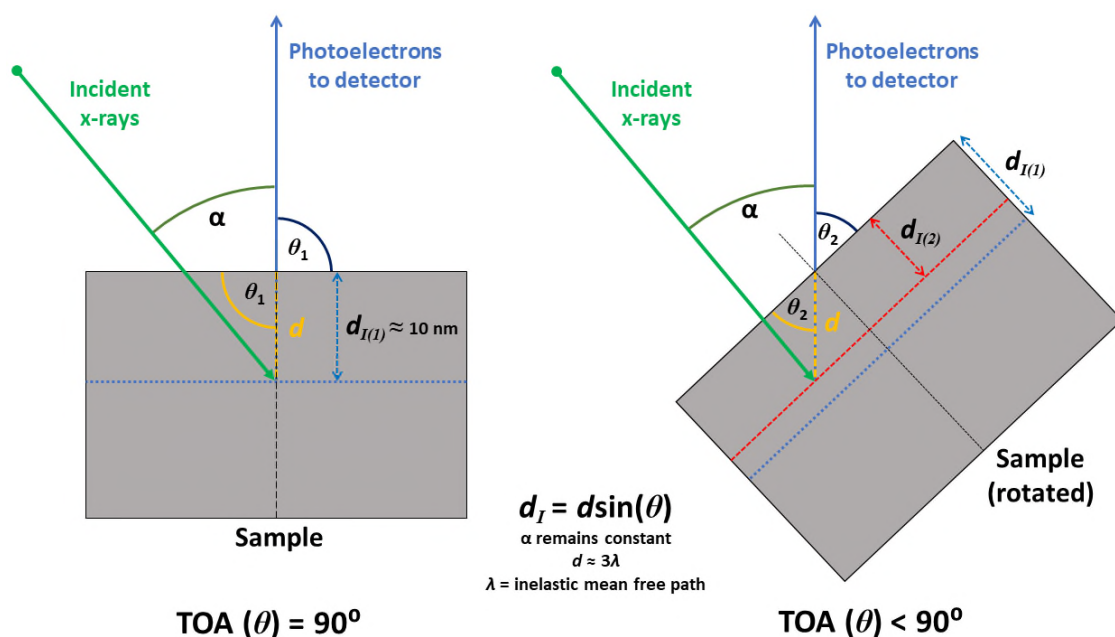


Figure 56: Diagram showing how information depth can be altered when using TOA-dependant XPS

A perpendicular scan will typically probe the first 10 nm of a sample⁸⁶. In this work, after the samples had been sputtered to the oxide/SiC interface scans with a TOA of both 90° and 15° were performed. At 15° the information depth is around 2.5 nm, hence is much more representative of the oxide/SiC interface.

CasaXPS software was used to model the measured XPS peaks. Each model included a number of components relating to different binding energies; these combined gave an envelope which closely matched the measured data. Figure 57 shows such a model for the 4-hour oxidised sample oxide/3C-SiC interface at a TOA of 90°, about the Si, C, and O peaks. Note that for the Si peak, the 2p orbital was observed and hence spin-orbit splitting was taken into account: for each compound a 3/2 and 1/2 peak was modelled.

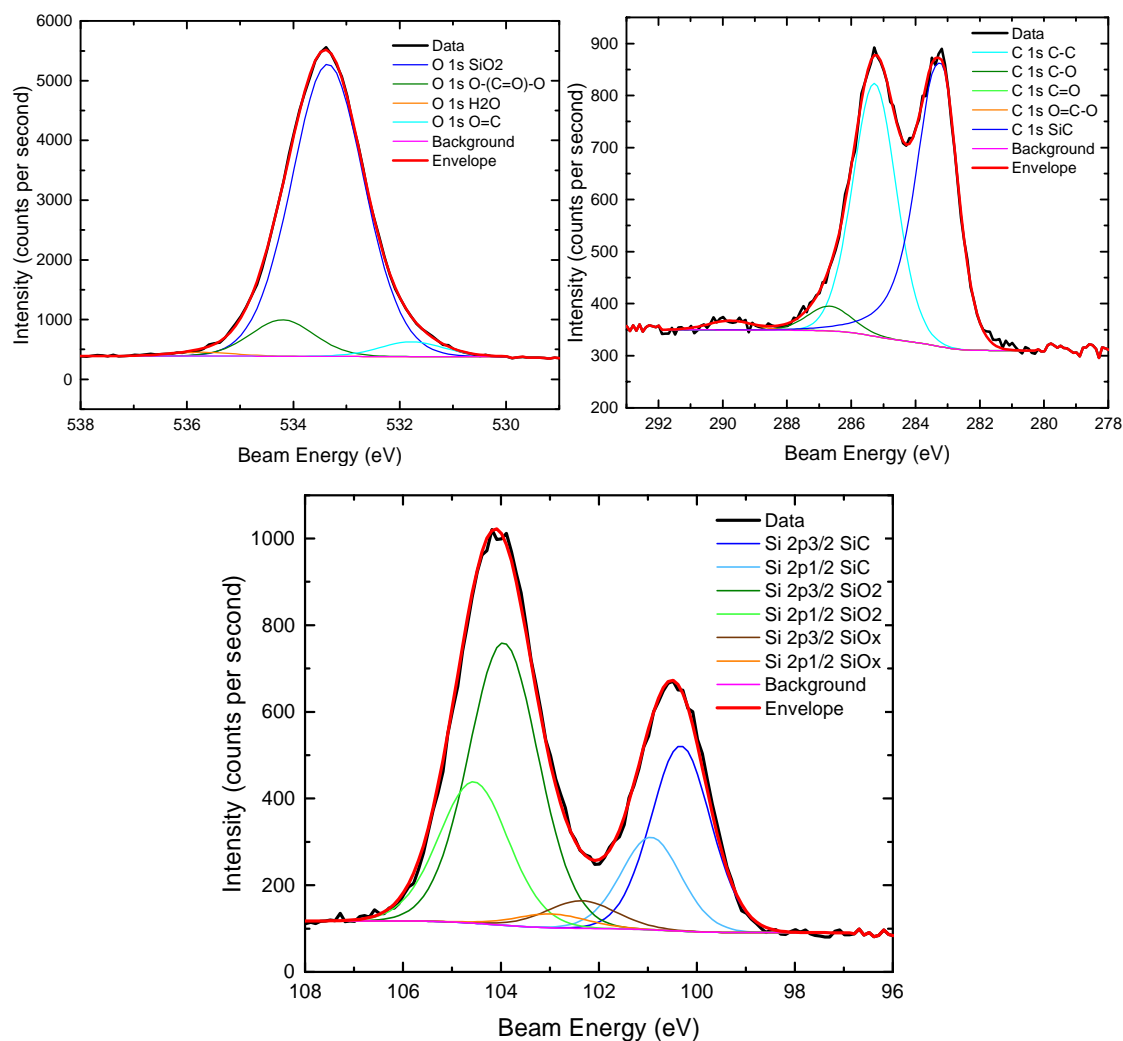


Figure 57: Model for XPS fitting showing component peaks about the measured O 1s peak (L), C 1s peak (R), and Si 2p peak (C)

The CasaXPS software was also used to quantify the amounts of each compound present within the sample. Most pertinent to this work is the SiO₂, SiC, and carbon-carbon bond (C-C) concentrations, which are shown in Table 1.

Sample	TOA	SiC %	SiO ₂ %	C-C %
17-625 4hr oxide surface	90°	1.31	92.64	1.84
17-625 4hr oxide/3C-SiC interface	90°	25.77	58.84	6.87
17-625 4hr oxide/3C-SiC interface	15°	5.55	56.71	25.93
17-625 6hr oxide surface	90°	0.47	93.95	1.99
17-625 6hr oxide/3C-SiC interface	90°	36.15	46.8	7.91
17-625 6hr oxide/3C-SiC interface	15°	6.33	53.48	26.66
17-625 10hr oxide surface	90°	0.3	94.41	1.72
17-625 10hr oxide/3C-SiC interface	90°	32.76	51.42	6.8
17-625 10hr oxide/3C-SiC interface	15°	4.07	62.93	21.28

Table 1: Relative concentrations of SiC, SiO₂, and C-C in samples with 4, 6, and 10 hour oxidation times. Estimated error is $\pm 4\%$.

As the data in Table 1 shows there is an abundance of C-C bonds present at the oxide/3C-SiC interface, which strongly suggests the presence of carbon clusters as suggested by Bassler et al.⁸⁷. The low-TOA data shows that total C-C concentration at the oxide/3C-SiC interface was approximately 25% across all samples, similar to that observed in thermally grown oxides on 6H-SiC and 4H-SiC⁸⁸⁻⁹⁰. It has been suggested by these authors that an effectively graphitic layer at the interface may form, which affects the channel mobility when MOS devices are fabricated. There was no appreciable difference in the C-C concentration with increasing oxidation time, suggesting that this concentration is independent of oxide thickness and oxidation time.

Table 1 also shows that the oxide is almost entirely composed of SiO₂, again with no significant dependence on oxidation time. Some sub-oxides were found to be present at both the surface and the oxide/3C-SiC interface, typically in concentrations less than 2%. It has been suggested that sub-oxides can act as interface traps in 3C-SiC and 4H-SiC⁹¹⁻⁹³, so these sub-oxides may be contributing to the D_{it} value calculated by electrical analysis (see section 5.2.2).

4.1.5 Secondary Ion Mass Spectroscopy (SIMS)

All Secondary Ion Mass Spectroscopy (SIMS) measurement in this work was performed by EAG Laboratories, a scientific services company based in New Jersey, USA. EAG also performed some data analysis, quantifying the amount of Si, O and C present in the samples.

SIMS is a destructive process which involves sputtering a sample by bombarding with high-energy ions and performing mass spectroscopy on the secondary ions emitted from the sample surface. The specifics of the technique are outside the scope of this work, but a comprehensive review of the technique can be found in A. Benninghoven et al.'s *Secondary Ion Mass Spectroscopy: Basic Concepts, Instrumental Aspects, Applications, and Trends*⁹⁴. SIMS is a very accurate characterisation technique, having a detection limit of 1×10^{10} to 1×10^{16} atoms/cm³. Such amounts are several orders of magnitude smaller than the measured quantities of Si, C, and O and so the error in this measurement is negligible.

For this work, individual scans for Si, C and O were performed in order to ascertain how the concentration of C varies within the oxide film. Figures 58-61 show the absolute values of Si, C and O for samples of varying thickness, along with a non-oxidised control sample.

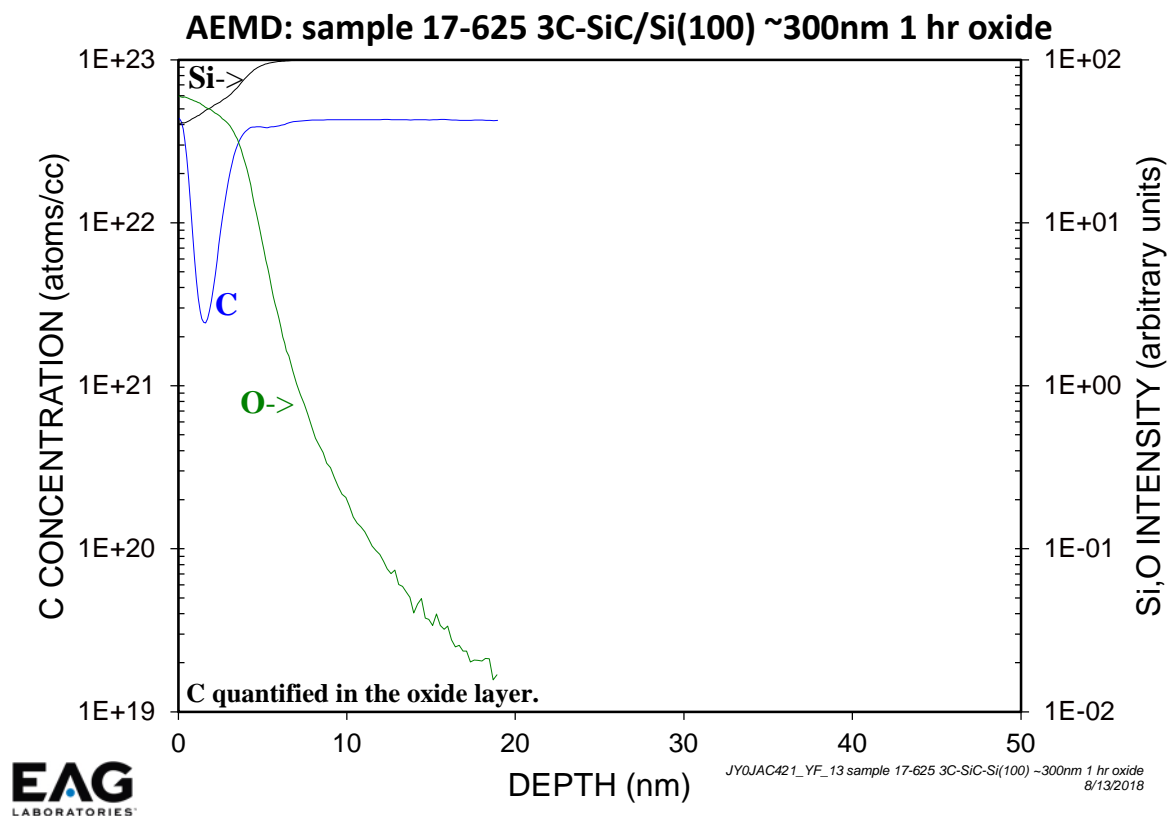


Figure 58: SIMS profile from samples oxidised for 1 hour.

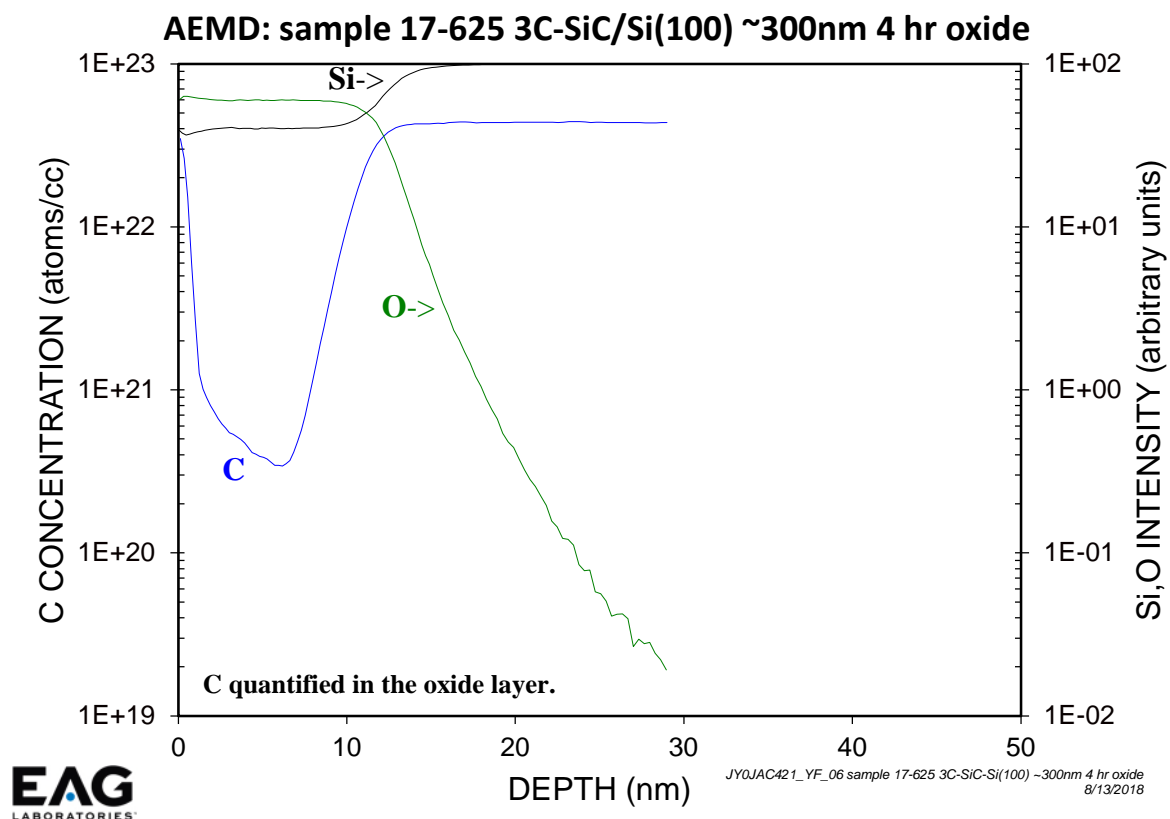


Figure 59: SIMS profile from samples oxidised for 4 hours

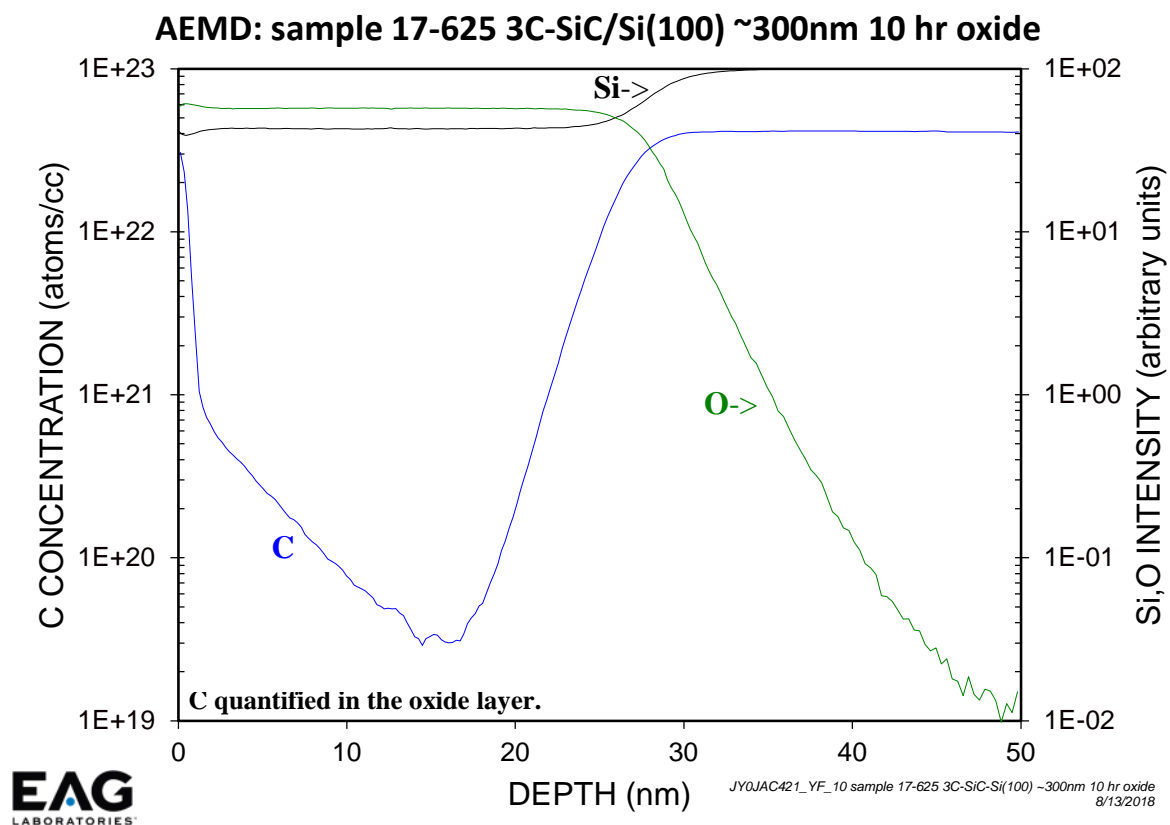


Figure 60: SIMS profile from samples oxidised for 10 hours

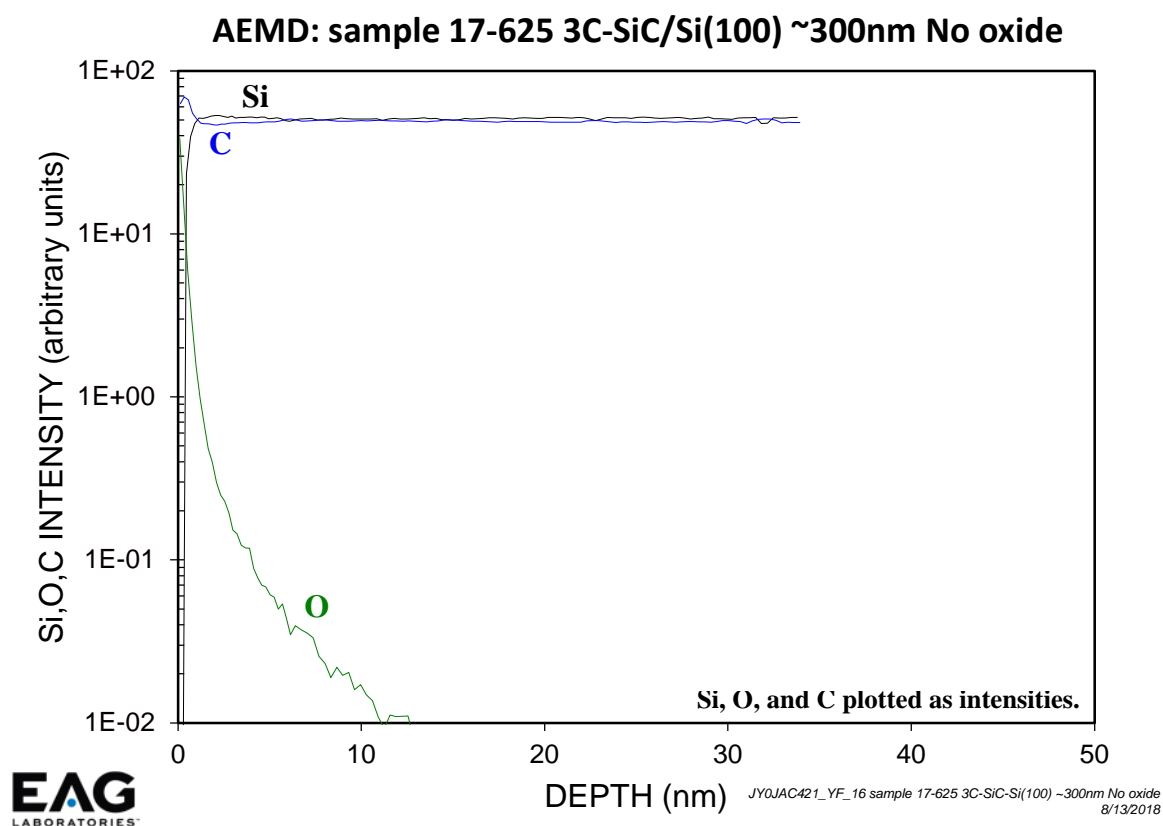


Figure 61: SIMS profile from the as-grown 3C-SiC.

These profiles suggest that there is carbon trapped at the oxide/3C-SiC interface, as the C concentration rapidly increases from approximately halfway through the oxide layer to its maximum concentration (i.e. the 3C-SiC epilayer). As the C concentration through the oxide varies, it must not be evenly distributed throughout the oxide. Clustering of carbon at the oxide/3C-SiC interface has been suggested by a number of sources ^{27,95} as has the transport of carbon out through the oxide as CO; see section 2.1. As the concentration of C at the interface does not exceed that of the 3C-SiC epilayer and the C concentration decreases with increasing oxide thickness, at least some of the C must be transported out through the oxide. Gavrikov et al. suggested that where C remains in the oxide it is likely to form either carbonyl defects ($\text{Si}_2=\text{CO}$) or carbon dimer defects ($\text{Si}_2=\text{C}=\text{C}=\text{Si}_2, \text{C}_2$). Respectively these will either release a CO molecule which can then transport to the oxide surface or grow further to form larger carbon defects, namely carbon clusters. A limitation of SIMS as compared to XPS is that SIMS provides no information about bonds, so from this data alone we cannot determine what form the carbon takes. When viewed in conjunction with the XPS data (see section 4.1.4) it appears extremely likely that the carbon observed is in fact graphitic and to be found in carbon clusters.

Assuming that the oxidation mechanism of 3C-SiC is qualitatively similar to that of 6H-SiC as described by Gavrikov et al., the same clusters would form in the oxide and at the oxide/3C-SiC interface. These C clusters may act as charge traps both at the interface and within the oxide itself ¹⁵. The relatively low D_{it} observed in this work suggests that despite the presence of these C clusters, they are not all electrically active. Some may however have contributed to the high current leakage through mechanisms such as trap-assisted tunnelling (TAT) ⁹⁶.

It should also be noted that the high concentration of C at the oxide surface of each sample (the air/oxide interface) is most likely atmospheric contamination rather than a true reflection of the C concentration at the surface of the oxide. There is however a noticeable increase in C concentration in the oxide as the air/oxide interface is approached.

4.1.6 Discussion

A number of physical characterisation techniques have been employed to characterise SiO_2 on 3C-SiC grown by dry oxidation at temperatures below 1000 °C. The purpose of this was threefold: to determine the thickness of the grown SiO_2 layers; to determine

whether the SiO₂ would change the surface roughness of the samples; and to determine whether C clusters would form within the SiO₂ layer which may act as trap sites.

XRR and X-TEM were used to determine the thickness of grown oxide layers and from this data growth rates could be extrapolated. As per the Song correction to the Deal-Grove model, there was shown to be a rapid initial exponential growth period which was followed by a linear growth period ⁵¹. The growth rate in this period was 4.08×10^{-2} nm/min around two orders of magnitude slower than oxidation of Si at the same temperature, and similar to the growth of SiO₂ on 4H-SiC at 950 °C. This growth rate is highly dependent on temperature, so future work could see a vast rate improvement by increasing the oxidation temperature by as little as 50 °C. The X-TEM data showed that the oxide layer was uniform, followed the surface morphology of the 3C-SiC epilayer, and did not appear to allow defects to propagate into the oxide layer.

AFM was used to assess the surface roughness of the SiO₂ layer alongside the as-grown 3C-SiC. The data shows clearly that the oxide neither smooths nor roughens the surface. Surface roughness was around twice as large as that previously achieved for 3C-SiC grown by heteroepitaxy at the University of Warwick, but with an RMS roughness of around 4.9 nm this was acceptable. Longer oxidation times (i.e. thicker oxide layers) did not appear to have an effect on the RMS roughness.

XPS and SIMS data both suggest that there is a significant concentration of carbon at the oxide/3C-SiC interface. This concentration does not appear to be dependent on oxidation time. XPS data showed the percentage of carbon directly at the interface to be approximately 25%, suggesting that in fact a graphitic layer is formed. XPS also showed that almost all of this carbon is found in C-C bonds, which again implies that a graphitic layer is formed. Several literature sources support the idea that carbon clusters form as part of the oxidation process, and while C-C bonds are also seen in low concentrations at the oxide surface, the majority of the carbon appears to remain trapped at the oxide/3C-SiC interface. This carbon may contribute to the interface state density, acting as charge traps. It may also contribute to trap-assisted tunnelling, causing current leakage through the grown oxide. A small amount of sub-oxide was also observed, which may further contribute to the interface state density.

5 Electrical Characterisation of 3C-SiC

5.1 Introduction

Recent work has seen interest in growing oxides on 3C-SiC for use in power electronics devices^{97,98}. While many investigations have been reported on the properties of the hexagonal polytype 4H-SiC, theoretically 3C-SiC may be more suitable for MOSFETs.

The oxide functioning as a dielectric is vital to ensuring that the MOSFET operates correctly, as without this no inversion region can be formed and the source and drain may not be electrically isolated from one another even with no applied gate voltage. The quality of grown oxides becomes even more important as devices become smaller, as the oxide layer will be necessarily thinner for smaller MOSFETs and so more prone to current leakage.

MOSFETs are a key technology in power electronics as they exhibit higher switching speed and lower power consumption than conventional BJTs⁹⁹. Several literature sources^{56,100} suggest that the smaller bandgap of 3C-SiC (2.4 eV compared to 3.265 eV of 4H-SiC¹⁰¹) allows fewer possible interface states, resulting in a smaller interface state density (D_{it}) and hence a greater field-effect mobility of electrons or holes in the inversion channel¹⁰². Another advantage that 3C-SiC's narrower bandgap provides is that smaller electric field strengths are required to switch a MOS-based device from accumulation to inversion, thus more power efficient devices can be made.

In addition to its inherent advantages for making MOS-based devices, 3C-SiC is the only polytype of SiC which can be grown heteroepitaxially on Si substrates (see section 1.5). As a result, 3C-SiC can be significantly cheaper and in mass volume to produce than 4H-SiC.

For industrial MOS-device production, SiO₂ is grown on Si wafers using a combination of wet and dry methods at temperatures between 900 and 1200 °C. Slow ramp rates must be employed to avoid thermal stress damage, making this process both time consuming and expensive. Wet or dry oxidation of SiC typically involves even higher temperatures (1000-1500 °C)¹⁰³ for both 4H- and 3C-SiC. It is common to use a variety of pre- and post-oxidation steps to increase the quality of the oxide and of the oxide/semiconductor interface. Principle among these techniques is the post-oxidation anneal (POA); this has been shown by Schoner et al. to improve D_{it} by as much as an order of magnitude for SiC

⁵⁶. The same work shows that that oxidation in a nitrogen-oxygen atmosphere can produce a smaller D_{it} , however nitrogen (N) is commonly used as an n-type dopant in SiC ¹⁰⁴. For this work it was important to ensure that no unintentional N-doping of the 3C-SiC occurred, and as such all oxidation was carried out in a pure oxygen (O₂) atmosphere. Other carrier gases such as Ar could be used to bring the overall cost down, however in this work concerns over the purity of the available Ar supply and potential incorporation of contaminants led to only pure O₂ being used.

It has recently been reported that high-temperature (1200-1400 °C) dry oxidation has produced homogenous SiO₂ on 3C-SiC ⁹⁷, however reducing the oxidation temperature while retaining high oxide quality and low leakage current is critical to ensure that 3C-SiC power electronics devices can be produced economically in large volumes. The quality of the oxide (SiO₂) produced is also vital, as poor-quality oxide layers with large numbers of mobile charges and high D_{it} will tend to have high leakage currents, which can limit their usefulness for device applications.

Typically, D_{it} of 1×10^{12} to 1×10^{11} cm⁻²eV⁻¹ can be achieved for SiO₂ on both 4H- and 3C-SiC epilayers by dry oxidation at temperatures exceeding 1120 °C and using processes which involve POAs ^{31,32,97}. Lower-temperature dry oxidation will in general cause a higher D_{it} , so there is scope to further refine the oxidation technique described herein.

5.2 Electrical analysis

5.2.1 Capacitance-Voltage (CV) measurements

Capacitance-voltage (CV) measurement is a powerful technique for analysing not only the capacitance of any fabricated MOS devices, but also assessment of the quality of the grown oxide, its thickness, and the presence and location of charge traps within the device ¹⁵. These CV sweeps can be used to extract measurements of oxide thickness, given by

$$W = \frac{K_s \epsilon_0 A}{C_{ox}} \quad (30)$$

where W is oxide thickness, C_{ox} is maximum oxide capacitance, K_s is the dielectric constant of the semiconductor (9.72 for 3C-SiC ¹⁰⁵), ϵ_0 is the permittivity of free space (8.85×10^{-12} Fm⁻¹) and A is the device area ¹⁵. This method was used in conjunction with

the other characterisation techniques detailed above to estimate the oxide thickness. Figure 62 compares the thickness measurements obtained from XRR, X-TEM, and CV data.

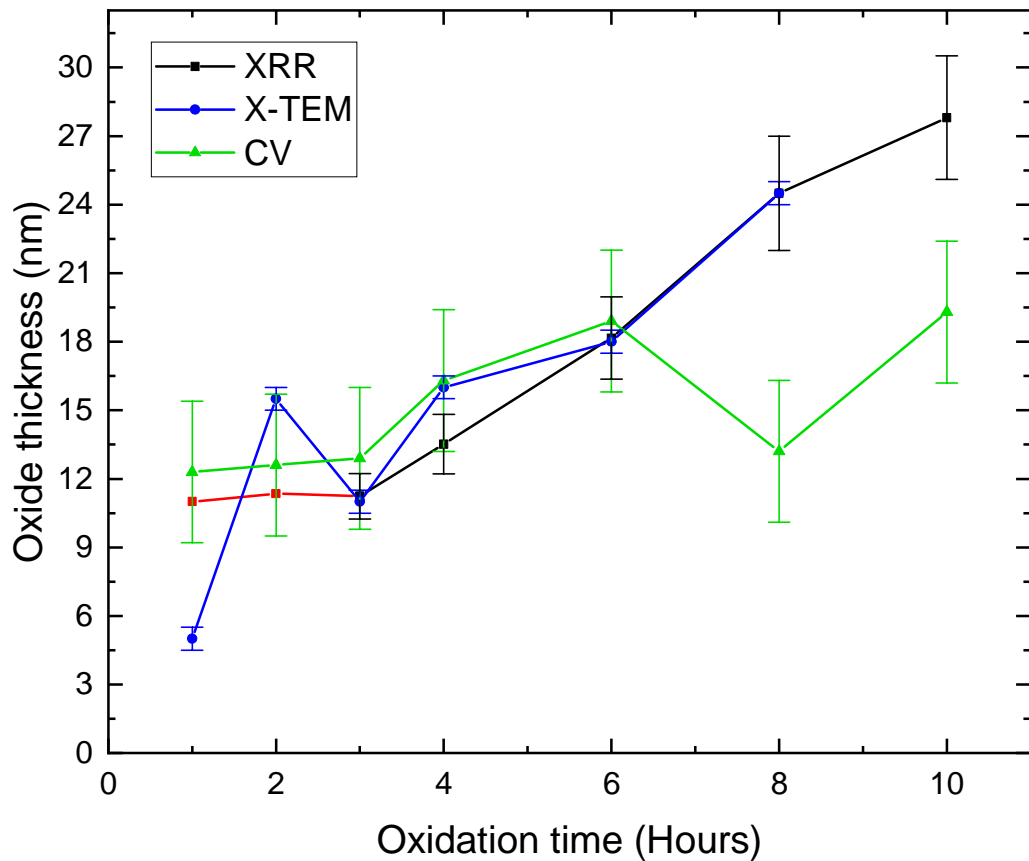


Figure 62: Oxide thickness as a function of oxidation time for XRR, X-TEM and CV measurements. Error bars are colour coded.

Correlation between the three thickness measurement techniques was generally good, excluding the obvious outliers at 1, 8, and 10 hours. The outliers in the CV data can probably be attributed to the inaccuracy in determining the maximum capacitance for the thicker oxide; a lower frequency CV sweep may have been required. For the samples of medium thickness (3, 4, and 6 hours of oxidation) a good correlation between measured thickness values from all three techniques is shown. At 3 and 6 hours all three data points were within the error ranges. As discussed in sections 4.1.1 and 4.1.2 the XRR and X-TEM thickness measurements are indicative figures rather than absolute thickness measurements, however the small deviation between all three techniques shown here suggests that, for these two oxidations times at least, the oxide thickness has been measured accurately.

CV measurements can also yield insight into D_{it} within the material. In this work the Castagne-Vapaille method was used to analyse D_{it} , which involves comparing the ratios of high- and low-frequency capacitance values and is given by

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{\frac{C_{LF}}{C_{ox}}}{1 - \frac{C_{LF}}{C_{ox}}} - \frac{\frac{C_{HF}}{C_{ox}}}{1 - \frac{C_{HF}}{C_{ox}}} \right) \quad (31)$$

where C_{ox} , C_{LF} and C_{HF} refer to the capacitance associated with the oxide in isolation, the low-frequency CV sweep, and the high-frequency CV sweep respectively¹⁰⁶. However, this was found to have a much larger error than the conductance method, which was also used to give an estimate of D_{it} – see section 5.2.2.

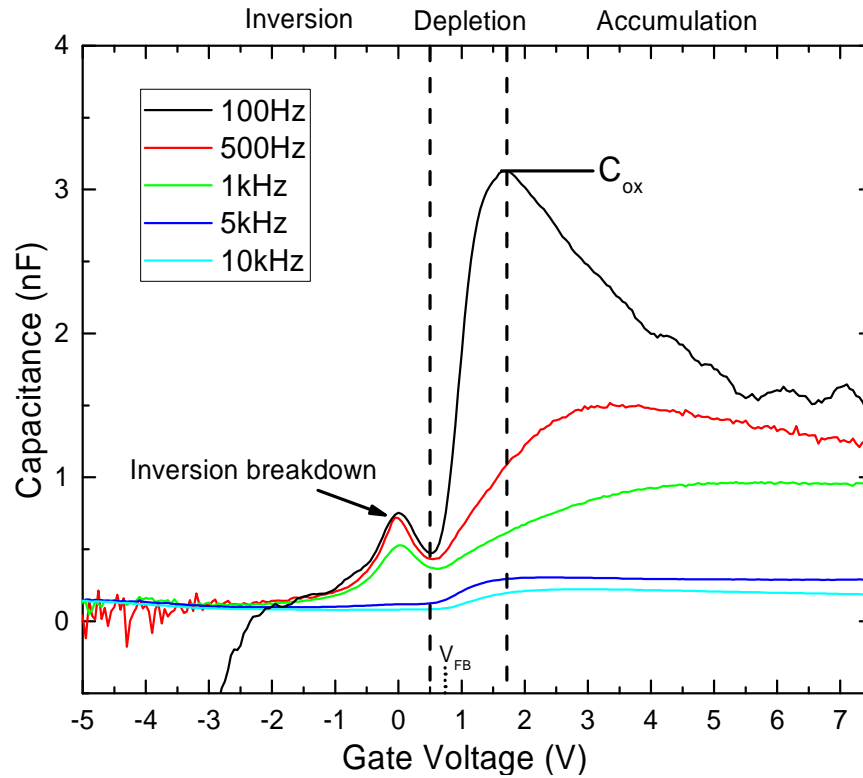


Figure 63: CV sweep of 4-hour oxidised sample (13.5 nm SiO₂) at room temperature (approximately 295 K). Some smoothing has been applied to the 100 Hz curve as noise dominated in strong negative biases. Note the secondary peak around 0 V; this is the inversion region which quickly deteriorates due to high current leakage through the oxide.

The CV data suggests that the 3C-SiC epilayers are lightly n-type doped, as the curve shown in Figure 63 is consistent with pMOS devices (so named as the inversion region contains p-type carriers). Any doping is unintentional and could be the result of contamination from an n-type dopant (such as N or P) during the CVD process. Dopant concentration is not expected to be more than $1 \times 10^{10} \text{ cm}^{-3}$.

Crucially this sample shows an inversion response, which has historically been difficult to achieve for 3C-SiC and equivalent wide-bandgap materials. This inversion response is small compared to the accumulation region and is quickly curtailed by the large leakage current when a negative gate voltage is applied. Minimising the leakage current or accounting for it within the measurement hardware may provide a full inversion region for study, as discussed below.

There is a large frequency dispersion in the accumulation region, which is likely the result of fixed charge traps in the oxide layer ⁸². Such charge traps could be external contaminants introduced during the oxidation process. Low-frequency (<10 kHz) measurements show the predicted carrier behaviour, however higher frequency sweeps are likely to be unreliable as the carriers will be trapped by the high density of fixed charge traps and at high frequencies would not have sufficient time to respond to the DC bias. This would result in carriers remaining bound to the trap sites.

Oxide thickness calculated using equation (1) from the room-temperature data corresponds closely with the thickness obtained from XRR analysis.

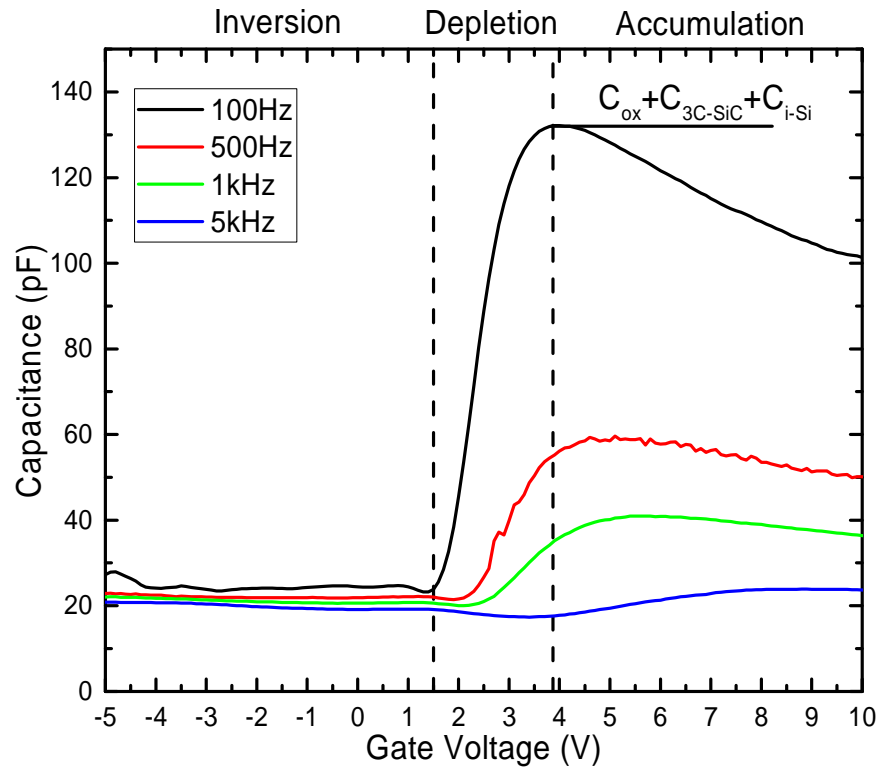


Figure 64: CV sweep of 4-hour oxidised sample (13.5 nm SiO₂) taken at 80 K. Some smoothing has been applied to the 100 Hz curve as noise began to dominate at high negative bias.

Figure 64 shows a CV sweep of the 3C-SiC sample oxidised for 4 hours (approx. 13.5 nm SiO₂) taken at 80 K. Again significant frequency dispersion is observed, indicating that

fixed charges are present in the oxide. The measured capacitance at low temperatures is much smaller than that at room temperature, suggesting that the effective dielectric layer of the MOS-stack is much thicker than at room temperature (see equation 1). Estimating the oxide thickness from Figure 64 supports this, as this suggests that this insulating layer is around 415nm; i.e. the thickness of the grown oxide, the 3C-SiC epilayer, and the i-Si layer combined. In this instance it appears that carriers are accumulating at the interface between the i-Si layer and the p^- substrate. It is likely that reducing the temperature of the material both freezes out charge traps and reduces the carrier generation rate such that there are essentially no available carriers in the 3C-SiC epilayer.

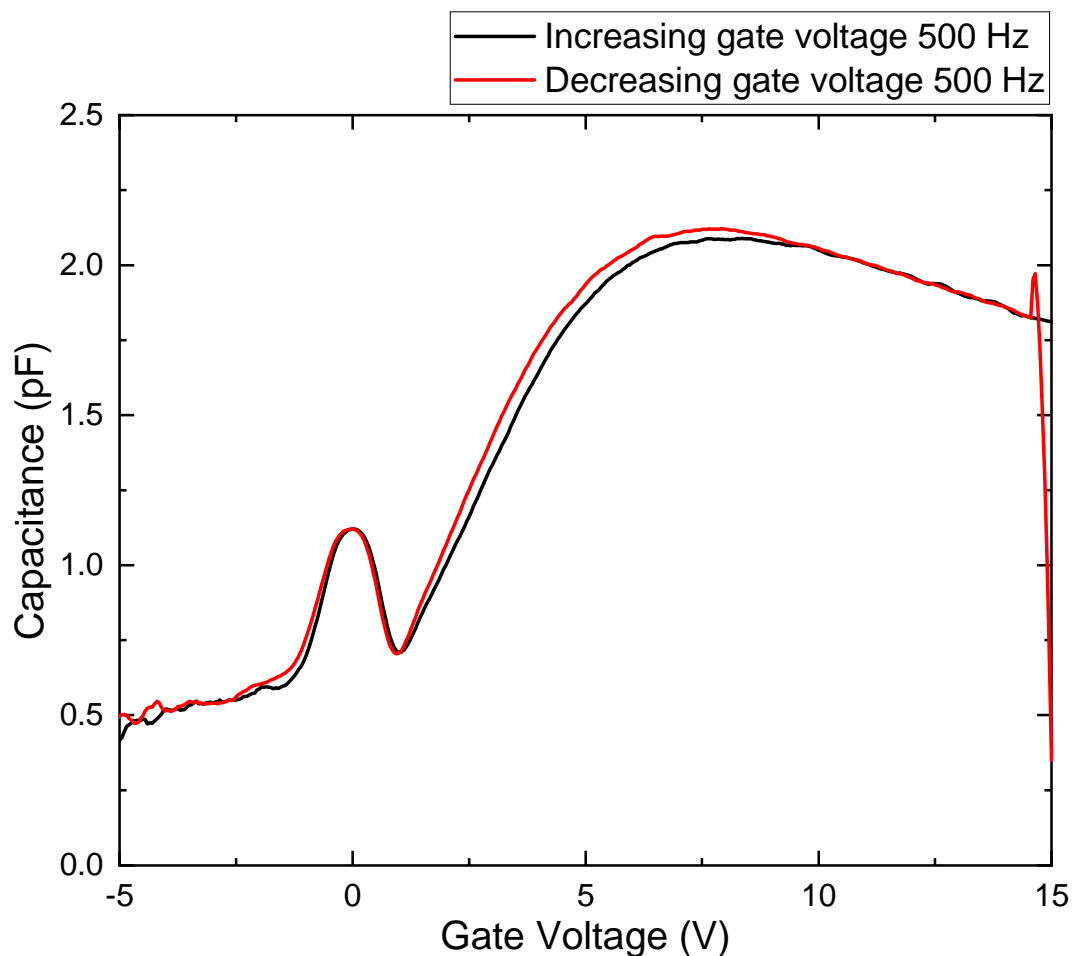


Figure 65: 500 Hz CV sweep of 3 hour oxidised sample taken at room temperature. Increasing and decreasing gate voltage sweeps are marked in black and red respectively. Some smoothing has been applied.

Hysteresis in the CV curves was very small. Figure 65 shows an example CV curve at 500 Hz with hysteresis which is representative for all samples. This is indicative of a lack of mobile charges in the oxide ¹⁵. It is not expected that near-interface traps (NITs) will significantly affect the behaviour of carriers as most NITs would be located high in the

conduction band of 3C-SiC ⁵⁶. As such they likely cannot accept carriers and so are effectively electrically inactive. The only charge traps of interest therefore are fixed charge traps and interface-state traps. The high quality of the grown oxide is likely due to the strict environmental and cleanliness controls in place during the wafer handling and oxidation processes. All wafer handling and oxidation took place inside an ISO 5 cleanroom, and the gases used for oxidation were of very high purity (6N O₂ and 9N N₂). This will have minimised any potential contaminants that could have either become incorporated into the oxide or diffused into the 3C-SiC.

The flatband voltage (V_{FB}) of the MOS stacks were determined by analysis of the C_{ox} and C_{HF} values as described by Schroder ¹⁵. For each sample, the gate voltage V_G was plotted against $1/(C_{HF}/C_{ox})^2$ and the second-order derivative of this curve taken. The peak of this derivative is found at V_{FB} . Calculated values can be found in Table 2. There was a large degree of variance in the flatband voltage and no clear trend.

Sample ID	Oxidation time (hours)	Oxide thickness (nm)	V_{FB} (V)	D_{it} (cm ⁻² eV ⁻¹)
17-625 1HR	1	5.0 ± 0.5	0.70 ± 0.05	5.9 × 10 ¹⁰ ± 4 × 10 ⁹
17-625 2HR	2	15.5 ± 0.5	0.75 ± 0.05	1.3 × 10 ¹⁰ ± 4 × 10 ⁹
17-625 3HR	3	11.0 ± 0.5	1.07 ± 0.05	8.5 × 10 ⁹ ± 5 × 10 ⁹
17-625 4HR	4	16.0 ± 0.5	0.62 ± 0.05	1.5 × 10 ¹⁰ ± 4 × 10 ⁹
17-625 6HR	6	18.0 ± 0.5	0.77 ± 0.05	8.75 × 10 ⁹ ± 5 × 10 ⁹
17-625 8HR	8	24.5 ± 0.5	0.07 ± 0.05	3.75 × 10 ¹⁰ ± 4 × 10 ⁹
17-625 10HR	10	27.8 ± 0.5	0.42 ± 0.05	1.5 × 10 ¹⁰ ± 4 × 10 ⁹

Table 2: Flatband voltage (V_{FB}) and interface state density (D_{it}) for all undoped samples. D_{it} was calculated using the conductance method. Thickness was taken from X-TEM data as this had the smallest margin of error.

The positive flatband voltage seen in all samples indicates that the interface state traps are positively charged, i.e. will trap electrons. Any POA treatment must therefore use an n-type SiC dopant to passivate these traps, such as N, P, or As. The simplest option would be to anneal the material in N₂ after the initial oxidation. This would pose a risk of unintentionally doping the 3C-SiC epilayer with N, as N is a common n-type dopant for SiC. Further study could ascertain the most suitable temperature for this anneal. Another

commonly used POA treatment is a thermal anneal in an inert and non-dopant gas such as Ar; reduction in the D_{it} value of up to an order of magnitude has been reported by this method⁵⁶. Schoner et. al. suggested that this was due to both the breakdown of π -bonded C clusters and the termination of dangling bonds of C atoms at the oxide/semiconductor interface, both of which would otherwise act as interface traps – this is discussed above in sections 4.1.4, 4.1.5, and 2.1.

5.2.2 Conductance-Voltage (G-V) measurements

Conductance-voltage (GV) measurements were carried out concurrently with all CV measurements. Conductance data is primarily of use in this instance to calculate D_{it} , using the conductance method as described by Nicollian and Brews⁸². In this method parallel conductance (G_p) is measured as a function of DC bias frequency (f) and plotted as G_p/ω against ω (where $\omega = 2\pi f$). The maximum value of this curve ($(G_p/\omega)_{max}$) is the reciprocal of the interface time constant τ_{it} . In practice an approximation of D_{it} is often sufficient and is given by

$$D_{it} \approx \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{max} \quad (32)$$

where q is the electron charge (1.6×10^{-19} C). Equation (2) has been used in this work to provide an estimate of D_{it} to within one order of magnitude.

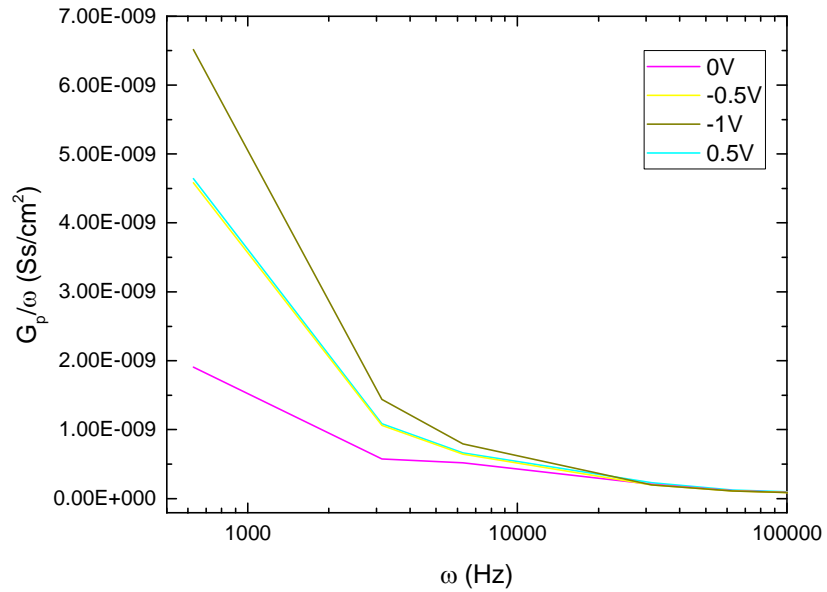


Figure 66: G_p/ω against ω for the 4 hour oxidised sample (16 nm SiO₂). The values below approximately 3 kHz are associated with oxide leakage current. D_{it} was calculated from the $\omega = 3$ kHz value at -0.5V, i.e. the onset of inversion.

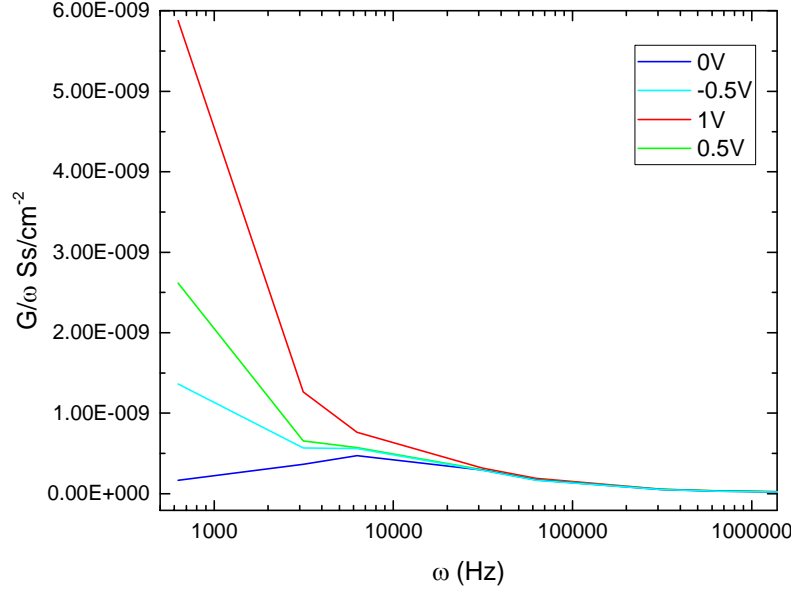


Figure 67: G_p/ω against ω for the 6 hour oxidised sample (18 nm SiO₂). The values below approximately 3 kHz are associated with oxide leakage current. D_{it} was calculated from the $\omega = 6$ kHz value at -0.5V, i.e. the onset of inversion.

Growth material	Oxidation temp. (°C)	POA	D_{it} (cm ⁻² eV ⁻¹)	Ref.
Si	1000-1120	None	1×10^9	102
3C-SiC	1120	None	1×10^{12}	56
3C-SiC	1120	1 hr in Ar at 800 °C	1×10^{11}	31
4H-SiC	1300	0.5 hr in O ₂ at 800 °C	1×10^{11}	32
3C-SiC	985	None	1×10^{10}	This work

Table 3: comparison of D_{it} values in this work and literature sources.

Figure 66 shows the plot of G_p/ω against ω for the 4-hour oxidised sample, for the end of depletion into the onset of inversion regions (0.5 V to -0.5 V). From this the value of $(G_p/\omega)_{max}$ was determined to be around 3 kHz on the -0.5 V curve (onset of inversion, the midgap). D_{it} was calculated from this to be approximately 1.5×10^{10} cm⁻²eV⁻¹.

The 6-hour sample (Figure 67) shows the characteristic peak expected in this plot, as described by the conductance method. As such we can make a much more accurate approximation of D_{it} . At the onset of inversion, -0.5 V, there is a peak at around $\omega = 6$ kHz, with a G_p/ω value of 5.6×10^{-10} Sscm⁻². This yields a D_{it} value of approximately 8.75×10^9 cm⁻²eV⁻¹, using equation 28.

D_{it} values 1-2 orders of magnitude larger have previously been achieved for both 4H- and 3C-SiC, however this requires both POA and often significantly higher growth temperatures, as shown in Table 3. For this work no POA has been performed. While this is a good indication of D_{it} it is only an estimate of the true value, although the true D_{it} is expected to be within an order of magnitude of this result. This is a significant improvement on previous work as even D_{it} of $1 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ is normally only achievable with both a higher growth temperature and some POA treatment. A full inversion region and better CV response at high frequencies should allow for a more accurate measurement of D_{it} . D_{it} values for all other samples can be found in Table 2.

The Castagne-Vapaille method¹⁰⁶ was also used to evaluate D_{it} and, for the 4hr sample, resulted in a value of around 3×10^9 . This was the lowest D_{it} value recorded for any samples measured. As with the conductance method this value can be taken as an approximation of the true D_{it} as this is far lower than expected as so is unlikely to be truly representative. This method is somewhat of a simplification and is only valid from the onset of inversion to a surface potential towards the majority carrier band edge¹⁵. The calculated value is taken from the onset of inversion; D_{it} will be at least an order of magnitude larger at the band edge. A more complete picture could be obtained if a strong inversion response can be measured- this is dependent on mitigating the leakage current which as discussed above could potentially be achieved with smaller device size. Doping the 3C-SiC epilayer may also improve the accumulation and inversion responses as a greater number of electrically active carriers will be available. Light doping (to around $1 \times 10^{17} \text{ cm}^{-3}$) should provide the most appropriate material for pMOS and nMOS devices.

5.2.3 Current-voltage (IV) measurements & leakage current

Current-voltage (IV) measurements were taken for all samples in order to ascertain the extent to which the oxides of various thickness showed current leakage. Samples were prepared in the same way as for all other electrical measurements (excluding Hall bars, see section 5.3) as described in section 2.3. All IV measurements were taken at room temperature in an electrically isolated dark box. While sweeping the gate voltage from low to high, the current was directly measured and the current density J calculated.

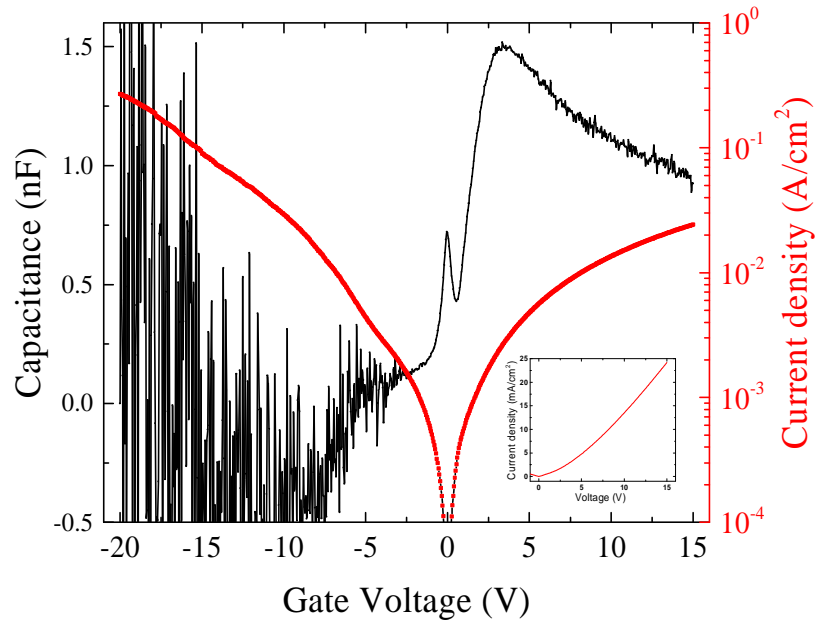


Figure 68: CV sweep for 4 hour sample (13.5 nm SiO₂) together with the normalised current density as a function of gate voltage for the same sample. A low bias frequency (500 Hz) was used for the CV sweep and shows overwhelming noise in the negative bias region. Inset is the 0-15 V region on a linear scale, showing the ohmic behaviour of the current in positive bias (i.e. low leakage current).

Figure 68 shows CV data together with the modulus of J for a sample with an oxide approximately 13.5 nm thick. It is representative of all samples; all showed a great deal of noise at low frequencies when a negative gate voltage was applied. The introduction of this noise correlates with the increase in the absolute value of J ; i.e. a significant increase in the oxide leakage current. This may also explain the collapse of the inversion region; while it is able to form at low inverse bias, quickly the leakage through the oxide is too great for minority carriers to accumulate at the SiO₂/3C-SiC interface. All samples also showed very similar current density profiles and there was no significant difference observed for oxides of different thickness. This suggests that longer oxidation times yielding thicker oxide are required to limit leakage current.

Interestingly, several samples showed a negative capacitance at gate voltages between approximately -5 V and -10 V, however they also showed a large amount of noise in this region. While there is some literature exploring negative-capacitance FETs as novel semiconductor devices, as they allow their channel surface potential to be amplified to levels greater than the applied gate voltage, further work is required to determine whether this negative capacitance is a true measurement of the devices present in this work or it is an artifact of an error in measurement^{107,108}.

SIMS data shows that there is a significant quantity of C at the oxide-semiconductor interface and distributed inhomogeneously throughout the oxide. Several literature sources

suggest that this C will form clusters which may act as charge traps -see sections 4.1.4, 4.1.5, and 2.1. As discussed in section 4.1.5 such clusters may contribute to leakage by way of trap-assisted tunnelling. The presence of C clusters within the oxide is a quantitative measure of the oxide quality; put simply, higher quality oxides will have less contamination.

Other current leakage mechanisms which may be contributing to the overall poor leakage performance of these devices include direct tunnelling and Fowler-Nordheim tunnelling^{16,17}. A much higher leakage was observed for the thinnest oxides, which can be attributed to direct tunnelling. In this process carriers tunnel directly through the energy barrier that the dielectric (i.e. the oxide) provides. This tunnelling current has been modelled for Si/dielectric gates using the Tsu-Esaki formula:

$$J = \frac{4\pi q_0 m}{h^3} \int_{E_{min}}^{E_{max}} TC(E_x, m_{diel}) N(E_x) dE_x \quad (33)$$

where m is the electron mass within the semiconductor, m_{diel} is the electron mass within the dielectric, $TC(E_x, m_{diel})$ is a transmission coefficient and the supply function $N(E_x)$ is defined as

$$N(E_x) = \int_0^\infty (f_1(E) - f_2(E)) dE_x \quad (34)$$

with f_1 and f_2 being functions which describe the energy distribution near the two dielectric interfaces¹⁰⁹. While the specifics of how much of the leakage can be attributed to direct tunnelling is of little impact to this research, it is important to consider that the influence of direct tunnelling greatly increases with a decrease in oxide thickness. This is simply due to the fact that a thinner dielectric layer will provide a smaller energy barrier for carriers to tunnel through, hence carriers can more easily direct tunnel through thinner oxides. As such, for any devices which would require a particularly thin oxide (in this work, shown to be less than 10 nm) one must consider further mitigating methods for current leakage wherever possible. One possible solution lies in exploiting one of the advantages of high-k dielectrics, which is that the oxide thickness can be increased while retaining the same capacitance for a given device. As detailed above a thicker oxide will typically mean a lower leakage current.

Using the photolithography techniques described in section 3.2, further work could see devices of a radius as small as 4-5 μm be fabricated on commercially available equipment.

In terms of industrial applications, similar but higher-resolution techniques such as e-beam lithography could potentially be used to further reduce device feature sizes to tens of nanometers in diameter ¹¹⁰. This combined with a relatively thick oxide layer may be sufficient to create functional devices with a low leakage current, however further research will be required to verify this.

5.3 Hall effect measurements of 3C-SiC epilayers

Alongside the oxidation study, some devices were fabricated from doped 3C-SiC in order to investigate some properties of the material: mobility, sheet resistance, charge density and Hall coefficient. Hall bars were fabricated from the heteroepitaxially grown 3C-SiC at a variety of dopant levels, as listed in Table 4. The structure of the fabricated Hall bars can be seen in Figure 69 below.

Sample ID	Structure	Dopants (doping level)
17-625	3C-SiC 300nm Si 100nm p-- Si (001) substrate	N/A
17-635	3C-SiC 50nm i-Si 100nm p-- Si (001) substrate	Boron ($1 \times 10^{18} \text{ cm}^{-3}$)
17-636	3C-SiC 50nm i-Si 100nm p-- Si (001) substrate	Boron ($1 \times 10^{19} \text{ cm}^{-3}$)
17-637	3C-SiC 50nm i-Si 100nm p-- Si (001) substrate	Boron ($5 \times 10^{19} \text{ cm}^{-3}$)
17-641	3C-SiC 50nm i-Si 100nm p-- Si (001) substrate	Phosphorus ($1 \times 10^{18} \text{ cm}^{-3}$)
17-642	3C-SiC 50nm i-Si 100nm p-- Si (001) substrate	Phosphorus ($1 \times 10^{19} \text{ cm}^{-3}$)

17-643	3C-SiC 50nm	Phosphorus ($5 \times 10^{19} \text{ cm}^{-3}$)
	i-Si 100nm	
	p-- Si (001) substrate	

Table 4: Structure and dopants of wafers used in this work.

The material was cleaved to squares of approximately $15 \times 15 \text{ mm}$ and the devices fabricated by a combination of photolithography, RIE, and various metal deposition techniques. Section 3 describes these processes in detail and provides a step-by-step walkthrough. The general process for fabrication of each device is well-established and has been used to make many similar devices in the past within the University of Warwick's Nano-Silicon group, however in each instance this was modified to suit the material under study.

5.3.1 The Hall Effect

The Hall effect is observed when a conductive material is placed within a strong magnetic field which lies perpendicular to the direction of current flow. In accordance with the right-hand rule, a resultant Lorentz force will act on the carriers within that material perpendicular to both the current and the magnetic field. In Figure 69 these directions are denoted by y , x , and z respectively. This will cause an imbalance of charge across the material as electrons and holes, influenced by this force, will accumulate on opposite sides of the material on the z -plane. This imbalance of charge is measured as a voltage across the width of the material, known as the Hall Voltage (V_H). V_H is often defined by the equation

$$V_H = \frac{IB}{qtp} \quad (35)$$

where I is current passed through material (A), B is the magnetic field strength (T), p is the hole density (cm^{-3}), q is the charge on an electron ($1.6 \times 10^{-19} \text{ C}$) and t is the thickness of the material under test. In the case of the Hall bar in Figure 69, this is the height of the mesa. From the Hall voltage various parameters of the 3C-SiC can be calculated: resistivity (ρ), carrier mobilities (μ_p and μ_n for holes and electrons respectively), carrier densities (p and n), and Hall coefficient R_H .

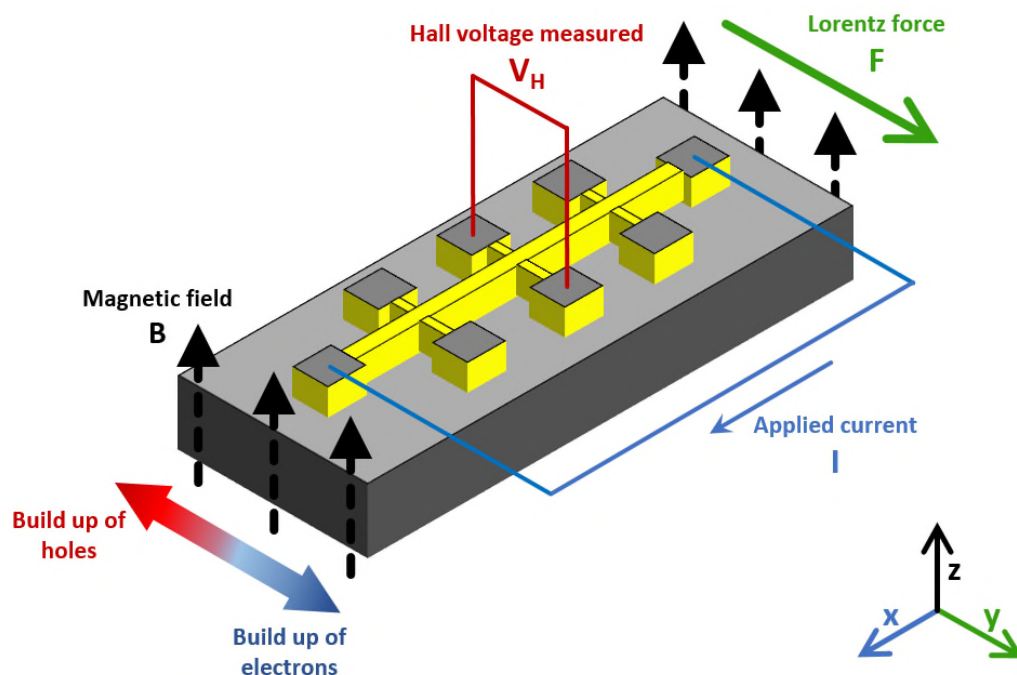


Figure 69: The Hall Effect as applied to a Hall Bar. Current flows in the bar in the $-x$ direction, magnetic field is in the z direction, resultant Lorentz force in the y direction.

The Hall bars fabricated as part of this research have been designed specifically for Hall effect measurements. Current is passed between the two endmost contact pads and the Hall voltage measured between pairs of oppositely oriented pads, as shown in Figure 69. Within the CCC the temperature of the device is then dropped in stages, and at each stage measurements of the Hall voltage are obtained. The polarity of the magnetic field is switched at each stage, so that any offset in the Hall voltage measurements can be eliminated – this offset can often be larger than the absolute Hall voltage. The various parameters are then calculated. Not only are these measurements useful for characterising the material and assessing its suitability for device applications, this data can also feed back into the epitaxy process to quantify the amount of electrically active carriers in the material and hence optimise growth processes.

5.3.2 Hall effect measurements

Regrettably, significant issues with the metal contacts prohibited the collection of any accurate CCC data and hence it was not possible to obtain any meaningful data from the fabricated devices. The main issue was that the metal deposited on the material did not make ohmic contact or was only ohmic at room temperature – see section 3.3.1. Once the CCC began to cool the devices, the IV sweeps became increasingly non-linear; Figure 71

shows this. Without an ohmic contact to the 3C-SiC the data is not reliable and hence no conclusions can be drawn about the behaviour of carriers within the material.

Thermal annealing of the contacts was attempted but was largely not successful as the contacts quickly oxidised (see section 3.3.5). While in several instances the contacts show an improved ohmic behaviour, the formation of a surface oxide prevented the adhesion of either Al or Au wires to the contacts when attempting to wire bond the devices to chip packages. The rough surface of the oxide also made attempting to take two-point IV measurements problematic, as some areas of the contact pads were suitably ohmic while others showed a very weak current response, suggesting that the surface oxide was acting as a dielectric.

Analysis of the Hall voltage measurements shows that even at room temperature the contacts are insufficiently ohmic. The CCC measures both the real and imaginary parts of the Hall voltage and calculates the phase angle with respect to the AC input current. The polarity of the magnetic field is reversed and another measurement taken; the mean can then be calculated. If this phase angle is 0° or 180° (i.e. the input and measured signals are in phase), this indicates that the contacts are ohmic. Any phase difference suggests charge build-up, and hence non-ohmic behaviour of the contacts¹⁵. Figure 70 shows the mean phase angle with respect to temperature for three of the samples.

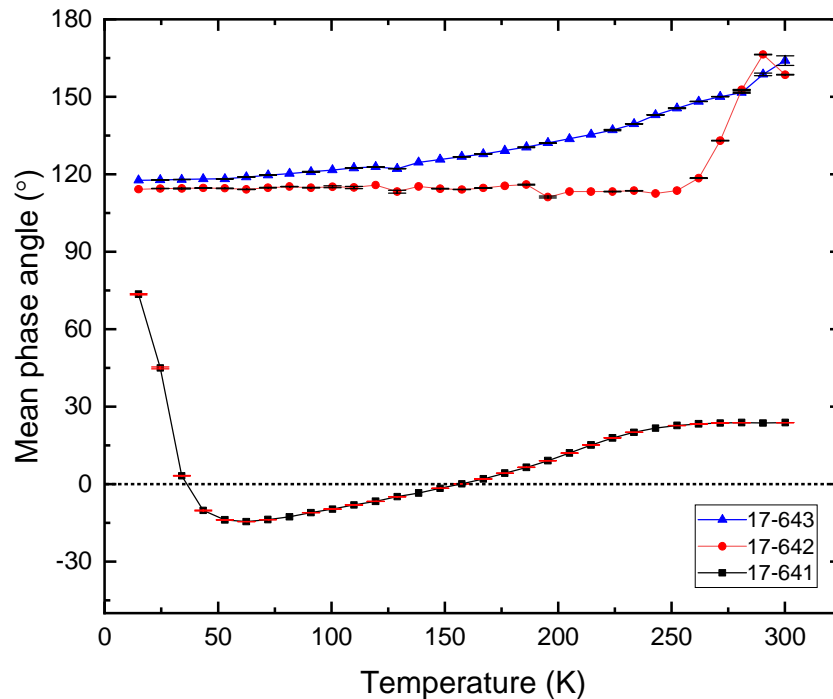


Figure 70: Mean phase angle of Hall voltage measurements as a function of temperature. Error bars are small.

From this data it is clear that the contacts start out as significantly non-ohmic and the signal move further out of phase with decreasing temperature. Although some points for all three samples are close to either 0° or 180° , the majority are substantially out of phase and hence the Hall voltage figures are totally unreliable. The error was small for all data points. Comparing IV data collected by the CCC to the two-point measurements collected before the devices were wire bonded into chip packages and these chip packages connected to the CCC by soldering suggests that the wire bonding and soldering further increases the problem with non-ohmic contacts.

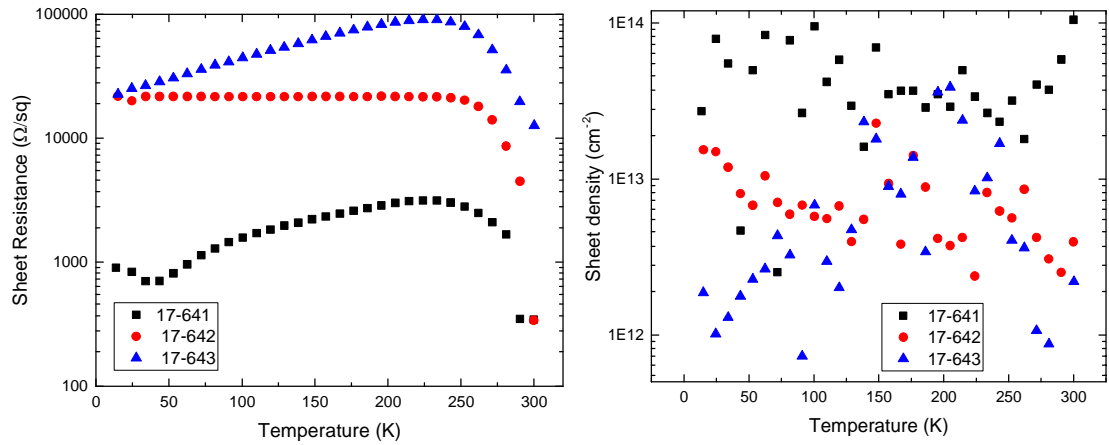


Figure 71: Hall parameters as a function of temperature: (L) sheet resistance and (R) sheet charge density. Non-ohmic contacts led to this data being unusable so no reliable temperature dependence of any parameter can be ascertained.

Data gathered from Hall effect measurements of the fabricated devices can be seen in Figure 71. As discussed above no conclusions can be drawn from this data as the contact pads quickly became too non-ohmic with decreasing temperature, however once the device fabrication issues described in section 3.3 can be overcome, measurement of these parameters should be elementary. This would form an excellent starting point for future research.

5.4 Discussion

Oxide layers of varying thickness were grown by dry oxidation atop 3C-SiC grown by heteroepitaxy on Si substrates. The 3C-SiC was of high quality and was grown using the low-temperature RP-CVD technique developed at the University of Warwick. Metal contacts deposited on the oxide layer formed MOS-stack devices, which allowed for electrical assessment of this SiO_2 . Current-voltage (IV), capacitance-voltage (CV) and conductance-voltage (GV) scans were performed at a range of frequencies between

100 Hz and 1 MHz at both room temperature and reduced temperatures down to 80 K. CV data was used to determine the thickness of the oxide, GV data to determine the interface state density D_{it} , and IV data used to assess the current leakage through the oxide layer.

Alongside fabricating MOS-stack devices, Hall bar devices were fabricated in order to assess the mobility, resistance, charge density, and Hall coefficient of the 3C-SiC epilayers. Significant issues were encountered during the fabrication process, mostly with thermal annealing of the metal contacts. Contacts were either not ohmic at reduced temperature or could not be annealed without producing a surface oxide which acted as a dielectric layer and inhibited analysis using the CCC. Further work would see these problems resolved and allow a complete analysis of the 3C-SiC epilayer, which itself would inform additional research into the material and its applications for power electronics.

For the oxide thicknesses calculated from CV measurements the error was relatively large. As discussed in section 5.2.3 the current leakage was very large which may be the reason for the inaccuracy in the calculated oxide thickness values. As such the CV data can also only be taken as indicative of the general growth trend. Improving the quality of the oxide layer may allow more precise values of thickness to be calculated using the same technique.

Taking all three data sets shown in Figure 62 together, an approximate growth rate can be determined, but it is clear that further work is required to improve the methodology and obtain more precise and accurate results. The first step would be to improve the quality of the oxide. An oxide which had a lower interface-state density and fewer C contaminants should have a much lower current leakage compared to the oxide grown in this work. From Figure 62 it is clear that in this work X-TEM was the most precise technique, however this has the disadvantage that it is destructive. Ideally the thickness measurement techniques should allow for devices to then be made from those samples, so that the exact oxide thickness is known (as there may be small variations between different samples). If the XRR technique could be refined and further calibration performed to ensure the data collected is both accurate and precise, this would be the most attractive for thickness measurement as it leaves the samples intact.

The results discussed herein indicate that there is scope for using the high-quality 3C-SiC on Si grown at the University of Warwick for MOS-based power devices, although the author suggests that dry oxidation at relatively low temperatures is a sub-optimal method for growing the oxide layer, and even a marginal increase in temperature would greatly reduce the oxidation time. The most important data is that of the interface state density D_{it} , as the calculated values are all around $1 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$, the same order of magnitude as many studies in which post-oxidation annealing has been performed. This work did not include any post-oxidation treatment, and literature suggests that POA can improve D_{it} by an order of magnitude^{56,100}. Thus, with very simple additional steps the devices could potentially be fabricated which exhibit D_{it} amongst the lowest previously observed for 3C-SiC. Further work is required to gain a more accurate D_{it} value, but the values herein are a reasonable estimate of the true D_{it} .

IV data showed that the current leakage through the oxide was relatively large, and this leakage is likely to have contributed significantly to the inability to maintain an inversion population at large negative bias. It has been suggested that C clusters within the oxide (formed as a by-product of the oxidation process) may be responsible for much of the leakage. X-TEM data showed that physical defects in the 3CV-SiC, such as stacking faults, did not appear to propagate through into the oxide layer. It is very important for most device applications to have a dielectric medium which is not leaky. The performance of this oxide could be greatly improved simply by increasing its thickness; at the temperature used for the oxidation in this work this would entail a significant increase in the oxidation time. An alternative would be to increase the temperature at which the samples are oxidised, which has been shown to greatly increase the rate of oxidation^{33,50,51}. This would also remove the issues encountered with using XRR to measure the oxide thickness for the very thinnest samples (see section 4.1.1), which would allow a more accurate determination of the oxidation rate. Other techniques such as FTIR could also be explored, either as techniques to directly quantify the oxide thickness or as calibration for other techniques (e.g. XRR).

6 Conclusions & further work

6.1 Summary of results

High-quality, fully relaxed 300 nm epilayers of undoped 3C-SiC were grown on an on-axis p⁺ Si (001) substrates 150 mm in diameter. This epitaxial growth was carried out by the reduced-pressure chemical vapour deposition method in an ASM Epsilon 2000 RP-CVD system, located in an ISO class 5 cleanroom^{39,40}. This epilayer was then oxidised by dry thermal oxidation in a conventional quartz oxidation furnace for lengths of time varying between 1 and 10 hours. All oxidation was at temperatures below 1000 °C. A number of these oxidised samples then had Al contacts deposited on the oxide surface by thermal evaporation to create simple MOS-stack devices.

The samples which did not have Al deposited on the surface were used for a number of physical characterisation techniques, in order to ascertain the oxidation rate of this material under these conditions; whether the oxide would cause additional surface roughness compare to the epitaxial 3C-SiC, and to determine the behaviour of carbon in the oxide layer (i.e. would it transport out during oxidation), as trapped carbon has been found to act as interface trap sites⁹¹⁻⁹³.

XRR and X-TEM were used to determine the thickness of the oxide layers and from this data a growth rate of approximately 4×10^{-2} nm/min was calculated. This growth rate is around two orders of magnitude slower than the growth of SiO₂ on Si and within an order of magnitude of the growth of SiO₂ on 4H-SiC by dry oxidation at similar temperatures³³. The X-TEM data also showed that the oxide layer was uniform, followed the surface morphology of the 3C-SiC epilayer, and that physical defects such as stacking faults and microtwins did not propagate into the oxide layer. AFM measurements showed that the RMS surface roughness did not change significantly with increasing oxide thickness, and that the RMS surface roughness of the oxide was the same as that of the 3C-SiC epilayer at around 4.9 nm. This surface roughness is within the expected range of 2-10 nm²⁵.

XPS and SIMS data strongly suggests that there is a significant concentration of C build-up at the interface between the SiO₂ and the 3C-SiC epilayer. TOA-dependant XPS showed a C concentration of between 21.28% and 26.66% through an information depth of around 2.5 nm, equivalent to approximately 6 monolayers of 3C-SiC. This concentration decreases with increasing distance from the oxide/3C-SiC interface. Longer oxidation times did not significantly affect the C concentration. XPS also showed that the

majority of this carbon is found to be C-C bonds, suggesting that graphitic clusters are formed. High-resolution imaging and spectral analysis techniques, such as scanning transmission electron microscopy (STEM) combined with energy-dispersive X-ray spectroscopy (EDX) or electron energy loss spectroscopy (EELS) could be used to identify this graphitic material (if present). Several literature sources have found this kind of carbon clustering at the oxide/semiconductor interface and it remains an ongoing challenge for SiC device fabrication⁸⁷⁻⁹⁰. Carbon at the interface may contribute to the interface state density (as discussed in section 5.2.2) and the carbon distributed through the oxide may be causing trap-assisted tunnelling, causing the high current leakage discussed in section 5.2.3.

Alongside this physical characterisation, the MOS-stack devices were investigated using capacitance-voltage (CV), conductance-voltage (GV), and current-voltage (IV) techniques. CV data was used to determine the thickness of the oxide, GV data to determine the interface state density D_{it} , and IV data used to assess the current leakage through the oxide layer. Critical among these results is the relatively low interface state density of around $1 \times 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$; this is within an order of magnitude of many studies in which post-oxidation annealing (POA) has been performed^{31,32}, and hence the expectation is that with POA this interface state density could be lowered by as much as an order of magnitude⁵⁶. An interesting continuation of this work would be to try POA or post-metallisation annealing (PMA) and determine the effect on the D_{it} value measured. It does appear that dry oxidation at temperatures as low as 1000 °C is a sub-optimal method for oxidising 3C-SiC, as seen by the high leakage current observed by IV analysis. As discussed above this leakage may have a link to the substantial carbon distribution throughout the oxide layer. X-TEM showed that physical defects in the 3C-SiC epilayer did not propagate through the material so this is unlikely to contribute to leakage. While reducing device sizes may go some way to mitigate leakage current, dry oxidising 3C-SiC at even marginally higher temperatures may lead to significant improvement in the quality of the oxide layer and is worth further investigation.

Hall bar devices were also fabricated from unoxidized material in order to assess the mobility, resistance, charge density, and Hall coefficient of the 3C-SiC epilayers. Significant issues were encountered during the fabrication process, which prevented the collection of any meaningful data. Thermally evaporated or sputtered metal (Al or NiCr) contacts were either not ohmic at reduced temperature or could not be annealed without

producing a surface oxide which acted as a dielectric layer and inhibited analysis using the closed-cycle cryostat (CCC) technique proposed to investigate these properties.

6.2 Suggestions for further work

First and foremost, further work should focus on overcoming the fabrication issues described in section 3.3.5, in order that Hall bars can be made to investigate the mobility, Hall coefficient etc. of the 3C-SiC epilayers. Given more time this work would have found the solution to these problems and so a complete picture of the carrier behaviour within the epilayer could be obtained.

Secondly, POA and PMA processes should be employed to investigate their effect on the interface state density, as if this could be reduced by an order of magnitude it would imply that the 3C-SiC grown for this work offers an attractive opportunity for power device applications. Any POA or PMA technique must employ an appropriate gas such that the trap sites are passivated; the author suggests N_2 as this has been shown to effectively passivate slow trap sites on 4H-SiC with an anneal around 1350 °C, by introducing N to the oxide/SiC interface ¹¹¹. Other options for POA include nitrous oxide (NO) and Ar, both of which have been shown to reduce D_{it} by as much as an order of magnitude on SiC ^{112,113}. Ar has been shown to break up π -bonded carbon (C) clusters and terminate dangling bonds of C atoms at the oxide/semiconductor interface, both of which reduce the number of available interface states. ⁵⁶

Another simple first step for future work would be to use lightly doped 3C-SiC (dopant concentration of around $1 \times 10^{17} \text{ cm}^{-3}$) and fabricate MOS stacks by the same oxidation method. The light doping should provide additional carriers which may make the electrical characterisation easier. Some preliminary work was done over the course of this project to investigate lightly doped 3C-SiC, however the initial data showed little of note and again time constraints limited further research. Overcoming the issues encountered with oxidation of metal contacts should carry over directly to this material, so complete characterisation of any doped material should be relatively straightforward. Being able to reliably oxidise doped material is crucial if this epitaxial 3C-SiC is to be used for any complex device applications (e.g. MOSFETs) as these devices will require both p- and n-type regions, either one of which may be 3C-SiC.

Finally, improving the oxidation would present an interesting area for future work. While the low-temperature method described herein is promising, the oxidation rate was relatively slow and so is probably unsuitable for wafer-scale production. Simply increasing the oxidation temperature would increase the oxidation rate, and as oxidation is so dependent on temperature^{33,50}, even a small increase in temperature (~ 50 °C) could dramatically reduce total oxidation time. Quantifying how higher oxidation temperatures affect the distribution of C within the oxide (and hence leakage and D_{it}) would also be an interesting avenue for further work as this may lead to optimisation of the oxide growth and hence make this epitaxially grown 3C-SiC suitable for a number of power device applications.

7 References

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